175-031

[redacted]

technical manual

MP MASTER
MA29720

ELDORADO

175-0310

Automatic Heterodyne

MICROWAVE FREQUENCY COUNTER

MODEL 988-7C

ELDORADO INSTRUMENTS COMPANY
2495 Estand Way
Pleasant Hill, California 94523
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JS-0510

LIST OF EFFECTIVE PAGES

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ADDENDUM

MODEL 988-7C

This Model is functionally the same as Model 988, except that the frequency coverage of each band is as follows:

Range 1: 20 Hz - 136 MHz

Range 2: 100 MHz - 825 MHz

Range 3: 0.825 GHz - 7 GHz

ELDORADO

This unit incorporates a module change as follows:

On the range 1 and 2 input amplifier board, the range two input amp gas been simplified to a high frequency input amp and divide by 4 integrated circuit. Board number: C-11-10732

The schematic of the new circuit has been installed in this manual in place of the sold schematic.

The input specification has been changed to the following:

Frequency range is now 100 MHz to 825 MHz
The dynamic range is -7 dBm to +10 dBm

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ERRATA

MODEL 988/989

Page ii line 4.3.8 change to read page "4-18"

Page iii line 4.4.6 change to read page "4-68"

Page v line 4-14 change to read "circuit type MC836 F, P, IC Data Sheet 4-32"

Page v line 4-27 change to read "circuit type SN74141,"

Page v line 4-28 change to read "circuit type SN74196,"

Page 3-1 Para. 3.2 line 5 place A1 in (A1)

Page 3-1 Para. 3.2 line 14 change to read "RF subsection. Listed in Table 3-1"

Page 3-3 Para. 3.2.1 line 3 change to read "1 (20 Hz to 136 MHz) operation, the direct counting technique is used, and the"

Page 3-4 left side line 2 change to read "amplified by an FET input amplifier and an ECL logic wide band"

Page 3-4 line 11 change to read "counter (1st DCU) and outputs the carry (clock) and 1-2-4-8 BCD via ECL-to-TTL translators to the counter PCB assembly"

Page 3-4 line 23 change to read "the inputted clock (carry) signal from the 1st DCU located on the A1A2 PCB assembly, storage of the counted data (BCD) and its conversion to decimal"

Page 3-4 Para. 3.2.2 line 3 spell "prescaler"

Page 3-4 line 21 change to read "scaled (divide by four) by an ECL counter"

Page 3-8 right side line 4 change to read "data is positive zone, positive true logic "1" = + 5V"

Page 3-14 right side line 22 change to read "duty cycle of the"

Page 3-17 right side line 13 & 14 change to read "from the 1.2 MΩ resistor (R7) effecting 1 MΩ input impedance."

Page 3-18 left side line 10 change to read "Figure 6-6, Range 2 Input Amplifier"

Page 3-18 right side line 16 change to read "Figure 6-6."

Page 3-19 left side line 17 change to read "Q16 is on. At this point assume."

Page 3-20 left side line 10 change to read "as a Decade counter"

Page 3-20 Para. 3.3.11 line 13 change to read "zero out the sweep"

Page 3-22 right side line 6 change to read "To pin 8 or U11, "

Page 3-22 right side line 20 change to read "500 KHz gated clock whose number of clock"

Page 3-22 right side line 27 change to read "A1A4 assembly Schematic Diagram, Figure 6-9 supports"

Page 3-22 right side line 47 change to read " 14), and the"

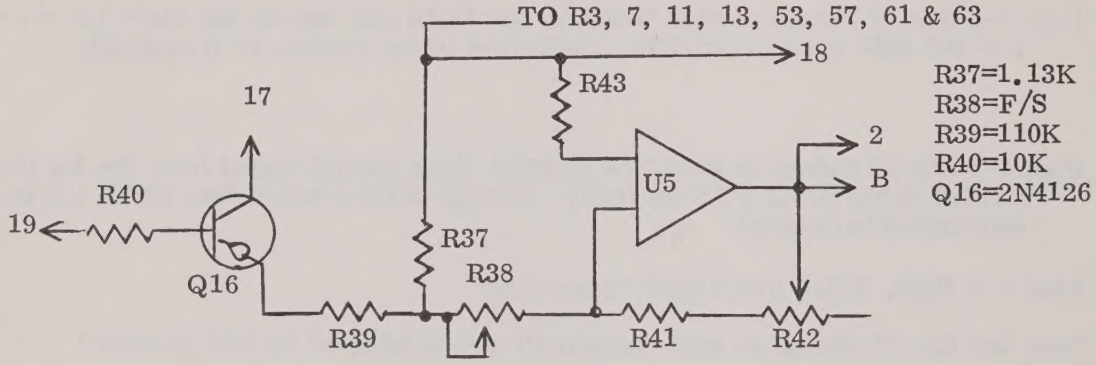
Page 3-23 left side line 10 change to read "output it's running count via"

Page 3-24 left side line 5 change to read "low, by inverter U1B, that gates off"

Page 3-24 right side line 5 change to read "(D/A) Converter is to provide an analog"

Page 3-25 Para. 3.3.13.3 change to read "The gain of the summing amplifier is adjustable by the SWEEP CAL adjustment potentiometer (R42). R42 is adjusted to provide an output ramp that will tune the YIG to it's upper limit when all 18 digital input bits are high. This control is set to provide a 13.4 GHz frequency limit for the Model 988 or 18 GHz for the Model 989.

Due to specification differences between individual YIG's a Sweep Pull Down Circuit is employed in some instruments. The following description is applicable to those units that employ this circuit.



SWEEP PULL DOWN CIRCUIT

When auto het lock-on is achieved a D/A STOP signal is generated by the Stop Detector Logic (part of A1A7) and applied at pin 19 to the sweep pull down circuit. This will initiate a pull down action decreasing the YIG tuning ramps amplitude by a small amount. R38 is adjustable to compensate for differences in individual systems and control the amount of pull down required. The pull down circuit function is to compensate for the YIG hystersis caused by the remnant magnetic flux which produces a small overshoot of the YIG tuning. The D/A Converter output"

Page 3-25 Para. 3.3.14 line 6 change to read "improvement of the YIG ramp control of the low end start"

Page 3-25 Para. 3.3.14 line 17 change to read "sisting of operational IC amplifier U1 and associated components. Control R13 called out"

Page 3-25 Para. 3.3.14 line 27 all units with serial number 746 and above Delete all the following "The BREAK control (R2) adjusts the voltage level applied to the non-inverting (+) input of operational amplifier U2 and sets the "break point" of the linearizer circuit----on the auto het chassis. Also delete Figure 3-8 on page 3-26."

Page 3-26 Para. 3.3.14.3 line 11 change to read "KΩ resistor (R17) and determines"

Page 3-26 right side line 5 change to read "to the figure 3-1 and 6-13 for the intercon-"

Page 3-26 Para. 3.3.15 line 4 change to read "The generation of the STOP, D/A STOP and LOCK command signals."

Page 3-28 left side line 12 change to read "at an offset by divider network R12, R5 and"

Page 3-28 right side line 36 change to read "(logic low) at U3 pin 6. The STOP signal"

Page 3-28 right side line 40 change to read "U3 and inverted generating the LOCK"

Page 3-28 right side line 42 change to read "Both the STOP and LOCK signals will"

Page 3-28 right side line 44 change to read "detected IF input signal remains IN"

Page 3-28 right side line 48 change to read "band detector indicates an out of band"

Page 3-29 left side line 3 change to read "high and effect the dropping of the command"

Page 3-29 right side line 21 change to read "(see figure 6-17 Power"

Page 3-29 Para. 3.3.17 line 4 change to read "circuit board (PCB)"

Page 3-30 left side line 14 change to read "pin 11 is connected"

Page 3-30 connector Table change to read

A6J1	1 MHz TIME BASE CLOCK	A2 Pad 8
A6J2	1 MHz AUTO HET CLOCK	A1A16 Pad 17
A6J3	1 MHz PHASE LOCK CLOCK	A1A12 input connector
A5J5	1 MHz Monitor/1 MHz Ext	External

Page 3-30 right side line 25 change to read "input $\overline{\text{PRESCALE}}$ and $\overline{10\ \text{Hz}}$ control"

Page 3-31 Figure 3-10 pad 40 change to read "$\overline{10\ \text{Hz}}$"

Page 3-31 right side line 11 change to read "pin 3 will be set to a logic high, providing the 10 Hz clock at U59 pin 6."

Page 3-31 right side line 21 change to read "$\overline{10\ \text{Hz}}$ control signal"

Page 3-32 left side line 3 change to read "10 Hz control signal"

Page 3-34 right side line 12 change to read "will latch up the eleven counter/Latches (U26-U30, U32-U35, U47 and U48) allowing the measurement"

Page 3-35 left side line 45 change to read "10^8 DCU (U20 pin 8)."

Page 3-35 right side line 27 change to read "gates (U38-U46 and U54)."

Page 3-36 left side line 31 change to read "data select gate (U67, U73 and U79A, B and C)."

Page 3-36 right side line 9 change to read "stretcher U52C and C2 its timing capacitor"

Page 3-37 Para. 3.3.19 line 2 change to read "(FIGURE 6-17)"

Page 3-37 right side line 16 change to read "volts at pad 5 to the linear"

Page 3-37 right side line 32 change to read "6-17 is located"

Page 4-22 Table 4-8 Step 7 line 2 change to read "provides the adjustment of A1A9Q3 tuned base circuit."

Page 4-44 change Figure number to "FIGURE 4-28"

Page 4-45 change Figure number to "FIGURE 4-29"

Page 4-46 change Figure number to "FIGURE 4-30"

Page 4-47 change Figure number to "FIGURE 4-31"

Page 4-48 change Figure number to "FIGURE 4-32"

Page 4-65 left side line 3 change to read "output. (refer to Figure 6-17 Power"

Page 4-65 right side line 13 change to read "pad 25?"

Page 4-68 left side line 16 change to read "4.4.6 Troubleshooting"

Page 4-69 center line 11 change to read "(Refer to Figure 6-6,"

Page 4-69 left side line 19 change to read "components. (Refer to Figure 6-6,"

Page 4-69 left side line 25 change to read "6-6, A1A1 assembly"

Page 4-69 left side line 28 change to read "or A1A1C32 (Refer to Figure 6-6, A1A1"

Page 4-70 left side line 5 change to read "$\overline{\text{ENABLE}}$ signal (Refer to Figure 6-7"

Page 4-71 right side line 2 change to read "at A1A4U11, pin 6? (Refer to Figure 6-9 the A1A4 Assembly Schematic Diagram.)"

Page 4-71 left side line 14 change to read "ure 6-16 the A1A13"

Page 4-72 Table 4-14 Step 3 line 2 change to read "6-16 the A1A13"

Page 4-73 Table 4-15 Step 2 line 4 change to read "Assembly A1A12. (Refer to Figure 6-15 A1A12 Assembly Schematic"

Page 4-73 Table 4-15 Step 3 line 4 change to read "(Refer to Figure 6-14 A1A11 Assembly"

Page 4-75 Table 4-17 Step 3 line 2 change to read "signal. If the 500 KHz clock is not present at A1A4U4 IC failure"

Page 4-77 Table 4-18 Step 1 line 6 change to read "1. A1A5Q15 Series regulator!".

Page 4-79 Table 4-18 Step 5 Add the following to Step 5 action paragraph "This action applies only to those units that utilize the D/A STOP signal and associated sweep pull down circuit as described in Para. 3.3.13.3 correction of this errata.

Page 4-80 Table 4-18 Step 5 (cont.) line 4 change to read "down is not noted a failure of A1A5Q16, R37, R38,"

Page 4-80 left side line 11 change to read "varies in amplitude"

Page 5-10 line C4, 5, 6 etc. in Ref. Column change to read "C4-6, 9-13, 15, 18;" in EE Part No. Column change to read "000158"

Page 5-10 line C16, 18 in Ref. Column change to read "C16"; in Qty Column change to read "1".

Page 5-10 line C17, 28 in Ref. Column change to read "C17, 14, 28" in Description Column change to read "Capacitor 22μF, 15 WVDC"; in the Qty Column change to read "3"; in the Mfr. Column change to read "SPR"; in Mfr. No. Column change to read "196D226X9015KA1"; in EE No. Column change to read "004645"

Page 5-10 line C26 in the Description Column change to read ".001 μF chip"; in the Mfr. Column change to read "CRL"; in the Mfr. No. Column change to read "N050FH102M"; in the EE No. Column change to read "003010".

Page 5-10 line C27 in the Description Column change to read "Capacitor, 220pf, Chip"; in the Mfr. Column change to read "SPR"; in the Mfr. No. Column change to read "10TS-T22"; in the EE No. Column change to read "006866".

Page 5-10 line C29, 31 in the Mfr. Column change to read "SPR"; in the Mfr. No. Column change to read "10TS-Q47"; in the EE No. Column change to read "006868"; in the Qty Column change to read "2".

Page 5-10 Add line C32 as follows:
"C32 Capacitor 2pF Mica SAN D155F020JO 000026 1".

Page 5-10 line CR1, 2, 3 in the Description Column change to read "Diode, HPA2800"; in the Mfr. Column change to read "HPA"; in the Mfr. No. Column change to read "HPA2800"; in the EE no. Column change to read "003067"; in the Qty Column change to read "3".

Page 5-10 line CR4, 5 in the Description Column change to read "Diode, FDH666"; in the Mfr. Column change to read "FAI"; in the Mfr. No. Column change to read "FDH666"; in the EE No. Column change to read "004471"; in the Qty Column change to read "2".

Page 5-10 line J1, 2, 3, 4 in the EE No. Column change to read "000433".

Page 5-10 line K1 in the EE No. Column change to read "006865".

Page 5-10 line Q3 in the EE No Column change to read "006862".

Page 5-10 line Q5, 6 in the EE No. Column change to read "006854".

Page 5-10 line Q9 thru Q25 in the Ref. Column change to read "Q7-25"; in the EE No. Column change to read "003265".

Page 5-10 line R3, 5, 13 in the Ref. Column change to read "R3, 13".

Page 5-10 Add line R5, after line R4, as follows:

"R5	Resistor, 1.8K, 1/8W, 5%	AB	BB1825	003143	1"

Page 5-10 line R6, 17, 18 etc. in the Ref. Column change to read "R6, 17-19"; in the Description Column change to read "Resistor, C.C., 510Ω, 1/8W"; in the Qty Column change to read "4".

Page 5-11 line R10, 11, 12 in the Qty Column change to read "3".

Page 5-11 line R21 in the Ref. Column change to read "R21, 34, 35, 54"; in the Qty Column change to read "4".

Page 5-11 Add line R41 after line R38 as follows:

"R41	Resistor, C.C., 56Ω, 1/8W, 5%	AB	BB5605	003132	1"

Page 5-11 Add line R42 after line R41 as follows:

"R42	Resistor, C.C., 1.2KΩ, 1/8W, 5%	AB	BB1225	003138	1"

Page 5-11 line R47 in the Description Column change to read "Resistor, C.C., 22Ω, 1/4W"; in the EE No. Column change to read "001071".

Page 5-12 line R48 in the Ref. Column change to read "R27, 48"; in the Qty Column change to read "2".

Page 5-12 Add line R51 after line R50 as follows:

"R51	Resistor, C.C., 10KΩ, 1/8W, 5%	AB	BB1035	001060	1"

Page 5-12 Add line U1 after line R52, 53 as follows:

"U1	Integrated Circuit Type MC10116	MOT	MC10116	006860	1"

Page 5-12 line U1 in the Ref. Column change to read "U2"; in the Description Column change to read "Integrated Circuit Type SC22904L and/or MC1690L"; in the Mfr. Column change to read "MOT"; in the Mfr. No. Column change to read "MC1690L and/or SC22904L"; in the EE No. Column change to read "006855".

Page 5-13 line C1, 4 thru 14 in the Ref. Column change to read "C1, 4-16"; in the Qty Column change to read "14".

Page 5-13 line C19, 20 in the Description Column change to read "Capacitor, 22μF, 15 WVDC"; in the Qty Column change to read "3"; in the Mfr. Column change to read "SPR"; in Mfr. No. Column change to read "196D226X9015KA1"; in EE No. Column chabge to read "004645".

Page 5-13 line R5, 6 etc. in the Ref. Column change to read "R5, 6, 25-29".

Page 5-13 line R21, 22 in the Ref. Column change to read "R21-24", in the Qty Column change to read "4".

Page 5-13 line R38, 39 in the Ref. Column change to read "R38-40, 42, 43".

Page 5-15 line C1, 3, 4 in the Ref. Column change to read "C1, 3, 4, 9-12"; in the Qty Column change to read "7".

Page 5-15 Add line C6, after line C5, as follows:

"C6	Capacitor, 2.2μF Tant	SPR	CSR13E225KM	000251	1"

Page 5-17 Add line R2, after line R1, as follows:

"R2	Resistor, C.C., 100K, 1/4W, 5%	AB	CB1045	001131	1"

Page 5-17 line R15, 15 in the Description Column change to read "Resistor, C.C., 4.7Ω"; in Mfr. No. Column change to read "CB4R75".

Page 5-19 line R1, 5, 9 in the EE No. Column change to read "005258".

Page 5-19 line R3, 7, 11 in Ref. Column change to read "R3, 7, 11, 15, 37, 53, 57, 61, 65".

Page 5-19 line R4, 8, 12 in Ref. Column change to read "R4, 8, 12, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 54, 58, 62, 66"; in the Qty Column change to read "18".

Page 5-19 Add line R6, 19, 56, after line R4, as follows:

"R6, 19, 56	Resistor, Metal Film, 243K, 1%	AB	RN55D2433F	005322	3"

Page 5-20 Add line R43, after line, R42, as follows:

"R43	Resistor, Metal Film, 4.99K, 1%	AB	RN55D4991F	005303	1"

Page 5-20 Add line R44 as follows:

"R44	Resistor, Metal Film, 2.49K, 1%	AB	RN55D2491F	005304	1"

Page 5-20 Add line R46 as follows:

"R46	Resistor, Metal Film, 16.2K, 1%	AB	RN55D1622F	005325	1"

Page 5-20 line R51, 55, 59 in the Description Column change to read "Resistor, Metal Film, 10K, 1%"; in the Mfr. Column change to read "AB"; in the Mfr. No. Column change to read "RN55D1103F".

Page 5-20 line R67, 68, 80 in the Description Column change to read "Resistor, C.C., 4.7Ω, 1/4W, 5%"; in the Mfr. No. Column change to read "CB4R75".

Page 5-21 line C4, 6 in the Mfr. No. Column change to read "196D226X9015KA1"; in the EE No. Column change to read "004645".

Page 5-21 line Q1 in the Ref. Column change to read "Q2".

Page 5-21 line U1 in the Mfr. No. Column change to read "LM307N"; in the EE No. Column change to read "005291".

Page 5-21 Add line U3, after line U1, as follows:

"U3	Integrated Circuit, Operational Amplifier	NAT SEMI	LM301AN	005318	1"

Page 5-21 line VR1, 2 in the Ref. Column change to read "VR1"; in the Description Column change to read "Diode, Zener 1N749A"; in the Mfr. No. Column change to read "1N749A"; in the EE No. Column change to read "000527"; in the Qty Column change to read "1".

Page 5-21 Add line VR2 as follows:

"VR2	Diode, Zener 1N757A	FAI	1N757A	000535	1"

Page 5-25 line C16 in the Mfr. No. Column change to read "196D226X9015KA1"; in the EE No. Column change to read "004645".

Page 5-25 line Q2, 3 in the Description Column change to read "Transistor, 2N4427"; in the Mfr. No. Column change to read "2N4427".

Page 5-25 Add line R6, after R5, as follows:

"R6	Resistor, C.C., 10Ω, 1/4W, 5%	AB	CB1005	001067	1"

Page 5-26 line C10, 15, 18 in the Ref. Column change to read "C10, 15"; in the Description Column change to read "Capacitor 5pF Mica Disk"; in the Qty Column change to read "2".

Page 5-26 Add line R11, after R9, as follows:

"R11	Resistor, C.C., 18K, 1/8W, 5%	AB	BB1835	003148	1"

Page 5-27 line C7 in the Ref. Column change to read "C10"; in the Description Column change to read "Capacitor 100pF"; in the Mfr. No. Column change to read "D155F101JO"; in the EE No. Column change to read "000079".

Page 5-27 line C8, 10, 12 etc. in the Ref. Column change to read "C8, 12, 14, 16"; in the Qty Column change to read "4".

Page 5-27 Add line C18, after C17, as follows:

"C18	Capacitor 10pF	SAN	D155F100JO	000034	1"

Page 5-27 line C18, 19 in the Ref. Column change to read C19, 20".

Page 5-27 Add the following lines, after J1, 2, as follows:

"L1, 2, 4	Inductor, Ferrite	FER	56-590-65/3B	001654	5"
"L3	Inductor, 3.3μH	DEV	1025-32	000663	1"
"L4	Inductor, 2.7μH	DEV	1025-30	000662	1"
"L5	Inductor, .47μH	DEV	1025-12	000653	1"
"L6	Inductor, 100μH	DEV	1537-76	000723	1"

Page 5-29 line C2, 3, 9 in the Ref. Column change to read "C2, 3, 8, 9"; in the the Mfr. Column change to read "SPR"; in the Mfr. No. Column change to read "196D226X9015KA1"; in EE No. Column change to read "004695"; in Qty Column change to read "4".

Page 5-29 line C4, 5 in Ref. Column change to read "C4, 7"; in the Description Column change to read "Capacitor, 15pF chip".

Page 5-29 line C6, 7 in Ref. Column change to read "C5, 6".

Page 5-29 line L1 in Mfr. No. Column change to read "1537-36"; in the EE No. Column change to read "000669".

Page 5-31 line C2 in the Mfr. Column change to read "CRL"; in the EE No. Column change to read "005991"; in the Qty Column change to read "1".

Page 5-31 line C3, 10, 12 in the Mfr. Column change to read "SPR"; in the Mfr. No. Column change to read "TG-S10"; in the EE No. Column change to read "000158"; in the Qty Column change to read "4".

Page 5-31 line C4 in the Mfr. No. Column change to read "196D106X9020JA1".

Page 5-31 line C15, 16 in the Mfr. No. Column change to read "196D226X9015KA1"; in the EE No. Column change to read "004645".

Page 5-32 line R52, 56, 61 in Ref. Column change to read "R52, 56, 58, 61, 65, 74".

Page 5-32 line R53, 55, 59 in Ref. Column change to read "R53, 59, 66"; in the Qty Column change to read "3".

Page 5-32 Add line R54, after line R53, as follows:

"R54	Resistor, C.C., 5.6KΩ, 1/4W	AB	CB5625	001111	1"

Page 5-32 Add line R69, after R68, as follows:

"R69	Resistor, C.C., 220Ω, 1/4W	AB	CB2215	001086	1"

Page 5-32 line R77 in the Description Column change to read "Resistor, C.C., 68Ω, 1/4W"; in the Mfr. No. Column change to read "CB6805"; in the EE No. Column change to read "001079"; in the Qty Column change to read "1".

warranty

Eldorado instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. The liability of Eldorado under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer and has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Eldorado shall have the right of final determination as to the existence and cause of a defect. In no event shall Eldorado be liable for collateral or consequential damages.

The instrument should be shipped prepaid with the return form attached to the packing container. When the instrument is repaired it will be returned to you best way prepaid.

This warranty is in lieu of any other warranty, express, implied, or statutory, and no agreement extending or modifying it will be binding upon Eldorado unless in writing and signed by a duly authorized officer.

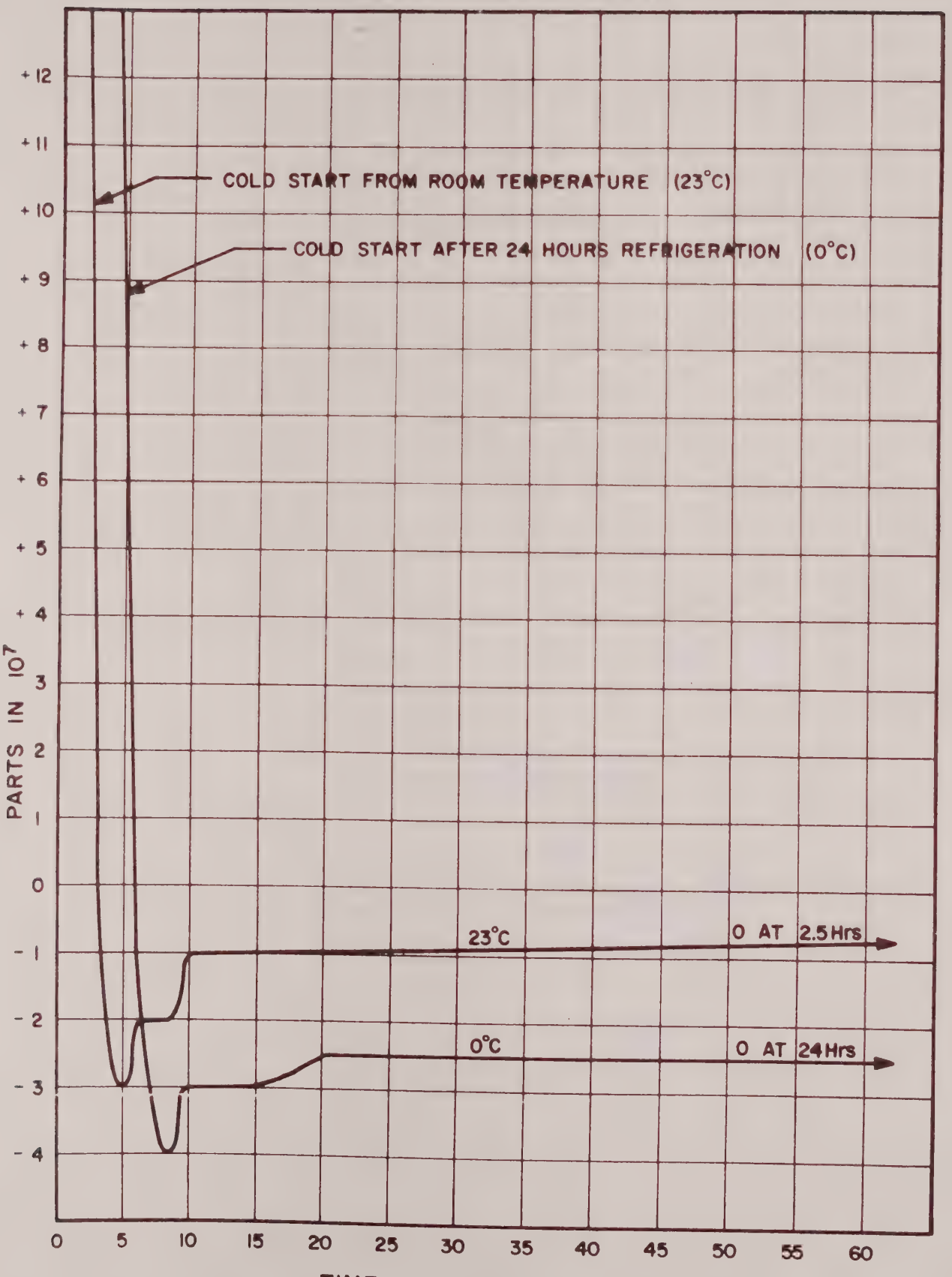
RECEIVING INSPECTION

Every Eldorado instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the instrument is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company. In any case where damage occurs in transit with the instrument in packing case, Eldorado's obligations under warranty are dependent on the customer's immediately notifying the carrier so that inspection can be made and a claim filed.

REPAIR SERVICE

Experienced service personnel and special test equipment are available at the factory to perform any necessary repairs. Every effort will be made to expedite the repair of instruments returned for servicing. Repair work will be performed only upon receipt of a written purchase order or authorization. Utilize the same procedure for returning an instrument for service as for warranty return. After receipt of the unit the Customer Service Department will issue a quotation of repair costs for your approval.

COLD START TESTS



C & C1 OPTION OSCILLATOR

The information necessary to complete this page appears on the serialized name plate located on the rear panel of the instrument.

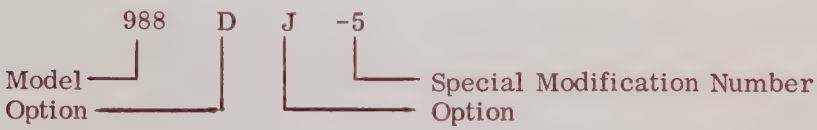
The manual is packaged with Model 988 Serial Number _____.
Model 989 Serial Number _____.

The following options are incorporated into this instrument.

Option C1	Option G1
Option D	Option J
Option D1	Option N
Option E	Option P
Option E1	Option R5
Option F	Option S
Option G	Option T

Special Modification Number _____.

Model Number and Option Legend



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SECTION 1

INTRODUCTION AND SPECIFICATIONS

SECTION 1

INTRODUCTION AND SPECIFICATIONS

1.1 INTRODUCTION

Features:

- Automatic operation.
- Frequency coverage to 13.4 GHz or 18 GHz.
- Resolution to 1 Hz.
- 11-Digit display.
- Input level monitor.
- BCD output (Option P).
- High FM immunity.
- Systems oriented.
- High stability time base.
- Display blanking.

The Models 988 and 989 Microwave Frequency Counters are completely automatic counters covering the entire range from 20 Hz to 18 GHz, 13.4 GHz for the 988, in a single instrument. These instruments consist of a direct counting 136 MHz counter whose range has been extended to either 13.4 GHz or 18 GHz by means of electronically programmed automatic heterodyne converters. The converter consists of a YIG (Yttrium-Iron-Garnet) - tuned Comb Generator that provides the comb power and frequency stability necessary to maintain the frequency accuracy fo the basic high stability clock. The Model 988 covers the range of 20 Hz to 13.4 GHz in three bands. Range 1, 20 Hz to 136 MHz, Range 2, 25 MHz to 625 MHz and Range 3, 625 MHz to 13.4 GHz. Ranges 1 and 2 are identical in both the Model 988 and the Model 989. Range 3 in the Model 989 has been extended to 18 GHz. Thus, the superior performance of heterodyne conversion for extending the range of digital counters is available in a completely automatic direct reading instrument with no fine tuning, manual tuning, interpolating or ambiguity.

Extending the range of frequency counters by heterodyne conversion is not new. In fact, manually tuned converters are used extensively at the present time. Since it is not susceptible to signal FM and takes the reading in the shortest possible sample time, it is by far the simplest and most straight forward technique. The Models 988, 989 have combined the performance of heterodyne conversion with the automatic programming capability and extremely wide bandwidth of its tunable YIG filters to provide a new standard of performance and convenience for frequency measurements. Signal acquisition is related to the comb generator sweep time which is about 50 milliseconds per GHz. However, once lock is achieved, readings are made continuously at a rate of 230 ms or as controlled by the Display Time Control.

Designed specifically for frequency measurements over a very wide range, the visual display consists of an eleven digit display that eliminates the need for time base, decimal point and measurement units switching that are necessary on most counters. Instead the display is conveniently sectionalized so that GHz, MHz, kHz and Hz digits are immediately apparent. To further simplify the display, blanking for all those digits of no interest or noisy signals is provided. Stored display providing a fixed readout during the measurement cycle, is also provided. Variable display time from 0.1 second to 10 seconds, independent of gate time, is available with automatic reset generated at the end of the display time. An infinite hold display time is switch selectable, maximum cw setting of time control, which also inhibits the automatic reset function. Remote reset is provided for via a rear panel mounted connector when option J is installed.

Resolution is 1 Hz, 10 Hz, 1 kHz and 10 kHz as a function of the Resolution/ Blanking switch using a fixed 1 second or 0.1 second time base gate. The 1 second gate provides 1 Hz resolution while the 0.1 second gate is used for all others.

Accuracy, $\pm$ 1 count $\pm$ oscillator stability, depends directly on the time base oscillator stability. The standard oscillator stability is 7 parts in 10^9 per day with optional oscillators available to increase stability to better than 1 part in 10^9 per day.

The 988/989 is basically a bench mounted instrument, for laboratory, production testing and varied frequency measurement uses. Front panel mounted, and well defined controls have been reduced to a minimum, which combined with simplified readout, make it particularly well suited for operation by unskilled personnel.

Greater versatility of the basic instrument is provided by addition of the above mentioned options, which are defined as Option D, E, or G for greater oscillator stability. Also available to further customize the instrument are: Option F, provision to preset the count chain for use in measuring local oscillator offsets and similar application; Option J, remote control of range selection and test function; Option N, rear panel mounted Input connectors; Option P, rear panel BCD data outputs; Option S, remote control of range 3 sweep frequency range; and Option T, 115/230 Vac, 50-60 Hz and 400 Hz operation.

1.2 COMPARISON WITH EXISTING FREQUENCY MEASUREMENT TECHNIQUES

The automatic heterodyne Frequency Counter provides the excellent electrical performance characteristic of the heterodyne converter with the convenience, wide frequency range, and direct readout capability of currently available automatic frequency measurement techniques. The heterodyne converter technique for extending the range of a basic low frequency counter has several important advantages over these other techniques. First, it is not susceptible to signal FM, and therefore, there is no need to be concerned about the FM content of the carrier to be measured. This is in marked contrast to the automatic transfer oscillator and automatic frequency dividers, where the amount of tolerable FM is specified with respect to both deviation and deviation rate. Secondly, the measurement of a desired frequency resolution is achieved in the fastest possible time; i.e., at 1 GHz, a 10 Hz resolution is achieved in 0.1 second with a direct heterodyne conversion, while the typical automatic transfer oscillator sample time for the same resolution is 2 seconds and the automatic divider takes 10 seconds. At 10 GHz, the heterodyne converter still takes only 1 second for a 10 Hz resolution, while the automatic transfer oscillator takes about 10 to 20 seconds, and the automatic frequency divider takes about 100 seconds. Input tracking for the currently available automatic frequency counters, which is the range that they can track the input signal without recycling, is about 2%, or 6 MHz at 300 MHz, 20 MHz at 1 GHz and 200 MHz at 10 GHz. The heterodyne converter, on the other hand, tracks the input over a constant range, about equal to the comb line spacing. A 200 MHz comb line spacing is used in the automatic heterodyne frequency counter.

The popularity of the heterodyne conversion technique is attested to by the large

number of heterodyne converter units that are in use. Until the introduction of the Model 988/989 however, heterodyne conversion had several practical limitations. The first limitation was the fact that the heterodyne converters, since they required mechanically tuned cavities, were limited in their frequency range. Therefore, several RF heads were required to cover the range from a few hundred MHz to 18 GHz. Also, these heads are quite expensive. The Model 988/989 uses only one YIG-tuned cavity to extend the range of the basic 200 MHz counter from 0.2 to 18 GHz.

Another disadvantage of the manual heterodyne converters is the fact that, since a considerable gear reduction is required to drive the tuning cavities, tuning is slow and tedious. In the 988/989 tuning is automatic, and the entire heterodyne converter range is scanned in about a second; no operator tuning is required.

A third disadvantage of the manual heterodyne converters, which is remedied by the 988/989, is that with the manually tuned cavities it is possible to tune to harmonics of the input signal unless the cavity is always tuned from the bottom of the range. The 988/989 always scans from the lowest frequency, thereby assuring that the frequency measured is correct.

Another disadvantage of the manual converter, is that it is necessary to add or subtract the counter reading to or from the tuning dial readout to obtain the correct frequency, a procedure that can easily lead to errors. This calculation is performed automatically in the 988/989 and no further manipulations are required. The advantage of the 988/989 over the manual heterodyne converters is that the frequency readout on the counter is direct.

The automatic heterodyne Frequency Counter, therefore, provides the technical superiority of the heterodyne conversion technique with the added advantages of fully automatic operation and direct frequency readout. This is provided at a lower overall cost than either the automatic transfer oscillator or the frequency divider techniques for comparable frequency coverage.

1.3 SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

Figure 1-1 is a functional block diagram of the Model 988/989 Automatic Heterodyne Microwave Frequency Counters. The range from 20 Hz to 136 MHz is coupled directly into the direct counter, whose input circuit consists of a wide band amplifier that accepts inputs over a dynamic range of 50 mV rms to 100V rms. This counter consists of a high-speed biquinary decade counter designed with ECL logic circuit elements to provide the maximum possible switching speed, followed by successive decades of TTL integrated circuits to drive the 11-tube display.

The time base control of the counter develops a sample gate of 100 milliseconds, thereby providing frequency readings at a maximum rate of 4 per second. For 1 Hz resolution, a 1 second gate is developed. A storage capability is provided for the BCD counters so that the readout time can readily be adjusted from a Hold setting to a maximum rate of 4 readings per second. This display readout control is independent of the gate time.

The Nixie tube display is an 11-digit readout in which the least significant digit reads in Hz. Over the entire frequency range each digit corresponds to the same unit of measurement; for example the fourth digit always measures from 0 through 9 kHz, the seventh digit always measures from 0 through 9 MHz, etc. Provisions have been made to blank the

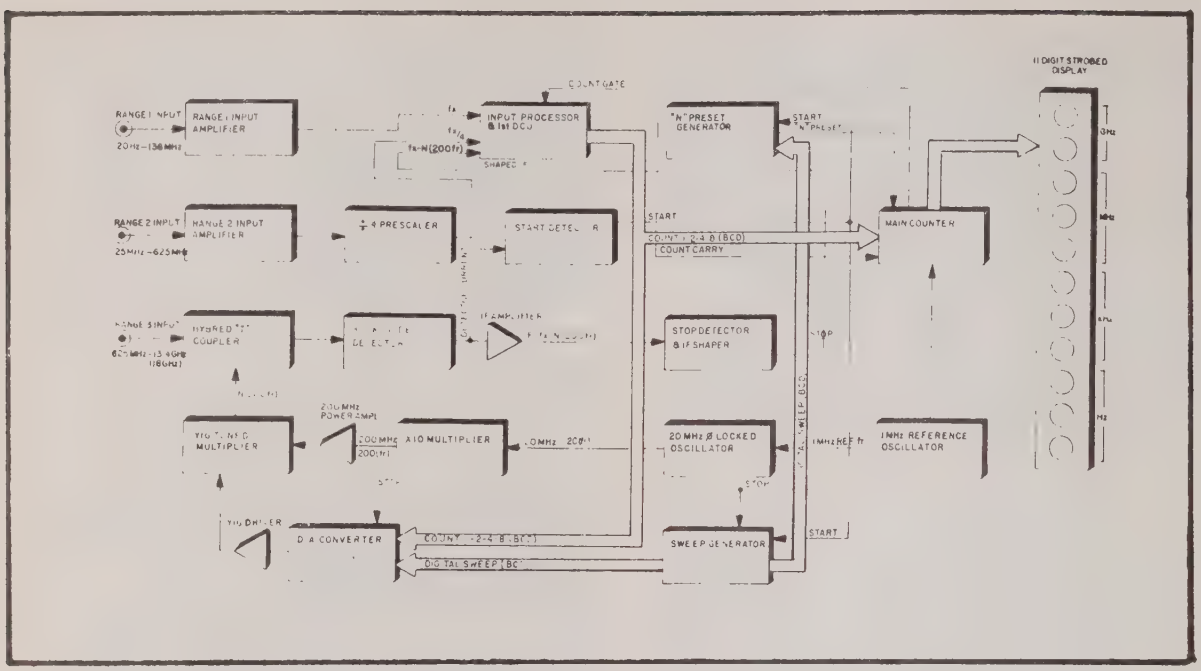


FIGURE 1-1

SIMPLIFIED BLOCK DIAGRAM

digits of no interest or from noisy unstable signals.

The basic accuracy and stability of the measurements are determined by a 1 MHz crystal-controlled clock with an aging rate of 7 parts in 10^9 per 24 hours. In addition to generating the required time base gate, this clock is multiplied to 200 MHz, where it serves as the driving signal for the comb generators of the YIG-tuned heterodyne converter. Frequency multiplication to 200 MHz is accomplished with a digital phase-lock technique, using high-speed integrated circuits, that provides signals with very low noise sideband and spurious signal contributions. This allows the generation of comb lines as high as 18 GHz with the spectral purity required to maintain the frequency accuracy of the 1 MHz crystal clock.

The heterodyne converter covers the range from .625 GHz to 13.4 or 18 GHz. The functional block diagram for either the Model 988 (13.4 GHz) or the 989 (18 GHz) are similar, the differences lie in the YIG multiplier assembly used. Operation is identical to conventional heterodyne converters except that the local oscillator being a YIG is tuned magnetically and is automatic in operation rather than a manually tuned cavity.

To illustrate the instruments operation assume that an input signal of 15,051,200,000 Hz is introduced into the heterodyne converter. The input signal if of sufficient amplitude will trigger the start detector which in turn will start the sweep generator and cause the YIG to scan in an upward direction, when the YIG outputs a 15.0 comb line a Het IF signal of 51.2 MHz is generated by the Back Diode Detector and is detected

by the stop detector circuit which generates a stop signal, that in turn will stop the sweep generator and the D/A converter. This action stops the YIG scan and locks the heterodyne converter to the 15.0 GHz comb line. When lock on is achieved the "N" preset generator logic identifies the "N" number as 150 by "looking" at the digital sweep BCD output and presets 150 into the three MSD of the counter. The first DCU counts the 51.2 MHz IF signal for a period of 100 milliseconds and thus adds the count to the preset number. The resultant is a direct counter reading of 15,051,200,000 Hz which is displayed on the 11 digit strobed display assembly.

TABLE 1-1 SPECIFICATIONS

FUNCTION	Digital microwave frequency measurements of inputs on three ranges.
Range 1, 50Ω: Range 1 1 MΩ:	Range 1 selects input range from 20 Hz to 136 MHz (988/989), with selection of 50Ω or 1 MΩ input impedance.
Range 2:	Range 2 selects input range from 25 MHz to 625 MHz (988/989).
Range 3:	Range 3 selects input range from 625 MHz to 13.4 GHz (988). 625 MHz to 18.0 GHz (989).
Test:	Self Test function counts internal time base oscillator as signal input and displays same.
SYSTEM TIMING	Range 3 - lock time 230 ms minimum, normally 50 ms/GHz up to maximum of 1 second. Once lock is established, reading may be every 230 ms.
INPUT CHARACTERISTICS	
Range 1:	20 Hz to 136 MHz.
Minimum Sensitivity (rms)	-13 dBm (50 mV rms) to 100 MHz. -07 dBm (100 mV rms) to 136 MHz.
Maximum Input (rms)	10V < 500 Hz; 5V > 500 Hz.
Maximum Input (rms) without damage	100V < 500 Hz; 10V > 500 Hz.
Nominal Input Impedance	1 Megohm 30 pF. or 50 ohms (selected)

Table 1-1 Specifications (Continued)

Input Coupling:	dc.
Connector:	Female type BNC, UG-912.
Range 2:	25 MHz to 625 MHz.
Minimum Sensitivity:	-7 dBm (100 mV rms).
Maximum Input without damage:	+27 dBm (5V rms).
Nominal Input Impedance:	50 ohms.
Input Coupling:	dc.
Connector:	Female type BNC.
Range 3:	0.6 GHz to 13.4 GHz (988). 0.6 GHz to 18.0 GHz (989).
Minimum Sensitivity (rms)	-7 dBm (100 mV rms) 1.1 GHz to 13.4 GHz; -3 dBm from 13.4 GHz to 18.0 GHz.
Maximum Input:	+10 dBm (0.7V rms).
Maximum Input without damage:	+20 dBm (2.2V rms).
Nominal Input Impedance:	50 ohms.
Input Coupling:	dc.
Connector:	Female precision type N/3 dBm Attn.
VSWR:	Typically 1.5:1.
RESOLUTION/TIME BASE:	Normal fixed gate at 0.1 second for 10 Hz - 10 kHz resolution and 1 second for 1 Hz resolution. Gate time for Range 2 are 4 seconds for 1 Hz and 0.4 seconds for 10 Hz through 10 kHz.
ACCURACY:	
Stability as a function of:	
Short Term:	7×10^{-9}/day after 30 days dynamic aging.
Long Term:	3×10^{-8}/week after 30 days dynamic aging.

Table 1-1 Specifications (Continued)

Repeatability:	1×10^{-7} after 48 hours warm up and 27 hours off time.
Phase Jitter:	Better than 5×10^{-9}.
Set Resolution:	$\pm 1 \times 10^{-7}$ multi-turn adjustment.
Adjustment Range:	± 10 parts per million minimum.
Temperature:	$\pm 5 \times 10^{-9}$/°C over temperature range of 0°C to +50°C.
Signal Output:	1 MHz, 2.4V peak-to-peak into 100Ω at rear panel mounted INT/MON BNC connector when T.B. Osc. switch is in INT position.
EXTERNAL OSCILLATOR	Switch selectable. Rear panel mounted selects either internal oscillator or use of an external oscillator.
Input Required:	1 MHz @ ≥1V rms.
Maximum Input:	5V rms
Input Impedance:	≃1k ohms.
Coupling:	ac.
Connector:	Female type BNC, UG1094/U.
VISUAL DISPLAY	
Numerical:	Eleven decades of in-line long life digital display indicators provide direct reading of all digits to 18 GHz, 13.4 GHz for 988.
Gate:	Gate lamp indicates gate on sample time.
Display Blanking:	Resolution/Blanking switch provides blanking of 1 kHz, 100 Hz, 10 Hz and 1 Hz display indicators.
Display Time:	Continuously variable from less than 0.1 second to approximately 10 seconds independent of time base gate time. Display time controls includes an infinite display time position.
Storage:	Display storage holds readings fixed between samples, updated automatically at the end of each measurement cycle.

Table 1-1 Specifications (Continued)

RESET	
Automatic:	After display time.
Manual:	Front panel pushbutton, overrides all function controls returns instrument to zero state.
Remote:	Momentary contact closure to ground applied to rear panel mounted connector resets the instrument when J option is installed. Also overrides the infinite hold setting of the display time control.
BCD OUTPUT (Option P)	Positive zone positive true logic, 1-2-4-8 BCD. "1" = +5V, "0" = 0V nominal. Rear panel 50 pin connector, Amphenol 57-40500.
ENVIRONMENTAL	
Operating:	+0°C to +50°C.
Storage:	-55°C to +80°C.
MECHANICAL	
Dimensions:	3.5 x 16.75" x 13" (H x W x D) without bail. 6" x 16.75" x 13" (H x W x D) with bail extended.
Weight:	Net 24.5 lbs., shipping 30 lbs.
POWER REQUIREMENTS	115 Vac ± 10%, 50-60 Hz. 130 watts nominal power.

TABLE 1-2 LIST OF OPTIONS

Option C1:	Temperature controlled crystal oscillator with the same stability as the standard oscillator for 230 Vac operation only.
Option D:	Internal temperature controlled 1 MHz crystal controlled oscillator. Provides oscillator stability of: Short Term: 5×10^{-10} peak-to-peak for seven minutes. Long Term: 2×10^{-9}/day after 48 hours warmup. Temperature: 2×10^{-10}/°C (avg.) from -0°C to +50°C. Retrace: $\pm 5 \times 10^{-9}$ of previous frequency after 60 minutes operation following 24 hours off-time.
Option D1:	Temperature controlled oscillator the same as Option D for 230 Vac operation only.
Option E:	Internal temperature controlled 1 MHz crystal controlled oscillator. Provides oscillator stability of: Short Term: 5×10^{-10} peak-to-peak for seven minutes. Long Term: 1×10^{-9}/day after 48 hours warmup. Temperature: 2×10^{-10}/°C (avg.) from -0°C to +50°C. Retrace: $\pm 5 \times 10^{-9}$ of previous frequency after 60 minutes operation following 24 hours off-time.
Option E1:	Temperature controlled oscillator the same as Option E for 230 Vac operation only.
Option F:	Positive and/or negative preset/offsets available for use in measuring Local Oscillator offset frequencies and similar applications. Permits presetting to any desired number from all zeros to 19999999000 in increments of 1 kHz. The preset number is determined by BCD coded wiring of 30 lines applied to the selected pins. Rear panel 50 pin connector, Amphenol 57-40500.

Table 1-2 List of Options (Continued)

Option G:	Internal temperature controlled crystal oscillator. Provides oscillator stability of: Short Term: 5×10^{-11} rms (for 1 second avg.). Long Term: 5×10^{-10}/day after 72 hours operation. Temperature: 2×10^{-10}/°C over range of 0°C to 50°C. Retrace: $\pm 5 \times 10^{-9}$ of previous frequency after 60 minutes operation following 24 hour off-time.
Option G1:	Temperature controlled oscillator the same as Option G for 230 Vac oscillator only.
Option J;	Remote control of test function and range selection by contact closure or saturated NPN transistors to ground. Remote control of display time by external 1 MΩ resistor.
Option N:	RF Input connectors mounted on the rear panel. A degradation of 2 dB from standard input specifications may be expected.
Option P:	Rear panel BCD data output, positive zone true logic, 1-2-4-8 BCD "1" = +5V, "0" = 0V nominal. 50 pin connector, Amphenol 57-40500.
Option R5:	Rack mounting.
Option S:	Remote control of range 3 sweep frequency range by contact closure to ground in 1-2-4-8 BCD form of the three most significant digits. Selection of the start sweep frequency (lower most frequency) and stop sweep frequency (upper most frequency) can be accomodated. Rear panel 24 pin connector, Amphenol 57-40240.
Option T:	Provides for 115/230 Vac ± 50-60 Hz and 400 Hz operation.

SECTION 2

INSTALLATION AND OPERATION

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section describes Incoming Inspection, Installation, and Operation of the Model 988/989 Microwave Frequency Counters.

2.2 INCOMING INSPECTION

Prior to packaging for shipment, this instrument received extensive operational, alignment and calibration tests, and was in perfect working order.

Upon receipt a visual inspection for damage incurred in shipment, and an inventory of the package contents as listed on the packing slip should be made. If the instrument has been damaged, notify the carrier immediately (see warranty).

2.2.1 Incoming Operational Check. The following procedure outlines an operational confidence check of the instrument without special tools, signal generators or special test equipment. The internal oscillator is used as the input signal and, therefore, does not test the high band heterodyne converters and associated circuitry. However much of the circuitry is inter-related and the test function provides a thorough confidence check.

a. See that the power ON/OFF switch is in the OFF position.

b. Connect the instrument power cord to the proper source.

c. Place the Power ON/OFF switch to ON.

d. Position the Display Time control to its minimum (full ccw) setting.

e. Place the Input switch to TEST.

f. Check out Display Blanking:

Place the Resolution/Blanking switch to 1 Hz. Note display reads 00 001 000 000.

Place the Resolution/Blanking switch to 10 Hz. Note display changes to 00 001 000 00-.

Place the Resolution/Blanking switch to 100 Hz. Note display changes to 00 001 000 0--.

Place the Resolution/Blanking switch to 1 kHz. Note display changes to 00 001 000 ---.

Place the Resolution/Blanking switch to 10 kHz. Note display changes to 00 001 00- ---.

g. This completes the operational confidence check.

2.3 INSTALLATION

The Model 988/989 is shipped for bench mounted operation with a self locking elevating bail installed. No special installation instructions are required. Plug the instrument into the appropriate ac power source and apply input signal (s) and the unit is installed.

2.4 OPERATION

Operation of the instrument is completely automatic after selecting the Input Range. A complete description of the front and rear panel controls, indicators, and connectors is supplied in Tables 2-1, and 2-2 are illustrated in Figure 2-1.

NOTE: The automatic heterodyne feature of this instrument is sensitive only to frequency changes. Therefore input signals below 625 MHz at levels below -7 dBm that effect a reading on the display are suspect. i.e., injecting 250 MHz at

-8 dBm can be accepted by the YIG circuits and will produce some output say 390 MHz. Since the YIG has locked on to what appears to be a good signal further changes in amplitude of the input signal will not cause the YIG to unlock and search for a new line. Even though the input level is increased, say to 0 dBm, the only way to break the lock is to change the frequency or manually reset (front panel manual reset only) the instrument.

TABLE 2-1

MODEL 988/989 FREQUENCY COUNTER

FRONT PANEL

CONTROL/INDICATOR/CONNECTOR	INDEX	FUNCTION
POWER	(1)	Power ON/OFF switch. Does not control oscillator oven power. As long as unit is connected to ac line oven power is applied.
DISPLAY Two Controls	(2)	
Time		Display time potentiometer and switch. Varies display time from 0.1 second to approximately ten seconds, instrument is automatically reset at the end of the display time. Also, in the full clockwise position switch is activated providing an infinite display time and inhibiting the automatic reset function.
Reset	(3)	Manual reset pushbutton. Overrides all controls and resets the instrument to zero.
RESOLUTION/BLANKING	(4)	Five position rotary switch selects the time base and provides blanking of the display.
1 Hz		Selects 1 second time base for 1 Hz resolution, all eleven digits displayed.
10 Hz		Selects 0.1 second time base for 10 Hz resolution, blanks the least significant digit. Units digit.
100 Hz		Selects 0.1 second time base for 100 Hz resolution, blanks the two least significant digits.
1 kHz		Selects 0.1 second time base for 1 kHz

Table 2-1 (continued)

CONTROL/INDICATOR/CONNECTOR	INDEX	FUNCTION
1 kHz (continued)		resolution, blanks the three least significant digits.
10 kHz		Selects the 0.1 second time base for 10 kHz resolution, blanks the four least significant digits.
GATE	(5)	Gate lamp provides visual indication of gate on sample time.
VISUAL DISPLAY	(6)	Eleven decades of in-line digital display tubes. Provides numerical readout of input frequency. Sectionalized into Hz, kHz, MHz and GHz decades. Unless blanked display is always in Hz.
INPUT	(7)	
Range/Test Switch		Five position rotary switch selects operating range or self test mode.
TEST		Applies the internal 1 MHz time base oscillator signal to the Range 1 input circuits. Does not test Range 2 or 3 input circuits.
RANGE 1 50Ω/RANGE 1 1M		Allows frequency measurements, from 20 Hz to 136 MHz, of input signals applied to the Range 1 BNC, with selection of 50 Ω or 1 MΩ input impedance.
RANGE 2		Allows frequency measurements, from 25 MHz to 625 Mhz, of input signals applied to the Range 2 BNC.
RANGE 3		Allows frequency measurements, from 625 MHz to 13.4 GHz on the 988 or to 18.0 GHz on the 989 of input signals applied to the Range 3 type N connector
NOTE: Signal input lines may be attached to the input connector at all times. The range switch connects only one input to the system at a time. Interlock switches allow only one mode of operation.		
RANGE 1 INPUT	(9)	Range 1 Input BNC.

Table 2-1 (continued)

CONTROL/INDICATOR/CONNECTOR	INDEX	FUNCTION
RANGE 2	(10)	Range 2 Input BNC.
RANGE 3	(11)	Range 3 Input N connector
INPUT LEVEL	(12)	Range 3 input level indicator. White range insufficient input. Green range adequate -7 dBm to +10 dBm input. Red range too much input.

TABLE 2-2 988/989 FREQUENCY COUNTER REAR PANEL

RANGE 1	(13)	Option N Range 1 input connector.
RANGE 2	(14)	Option N Range 2 input connector.
RANGE 3	(15)	Option N Range 3 input connector.
SWEEP PRESET	(16)	Option S Remote Range 3 Sweep Frequency range connector.
1 MHz		Internal External Oscillator selection.
INT/EXT Switch	(17)	Slide switch selects either internal reference oscillator or external.
INT/EXT Connector	(18)	BNC connector for injection of reference oscillator when in the external mode or for monitoring of the internal oscillator when in the internal mode.
PRESET/REMOTE	(19)	Option F and Option J connector.
DATA OUTPUT (Option P)	(20)	BCD digital data output connector.
POWER	(21)	Power cord receptacle.
115/230	(22)	115 V ac/230 V ac selector switch.
2 A.S.B.	(23)	Fuse holder, with 2 Amp SB fuse.

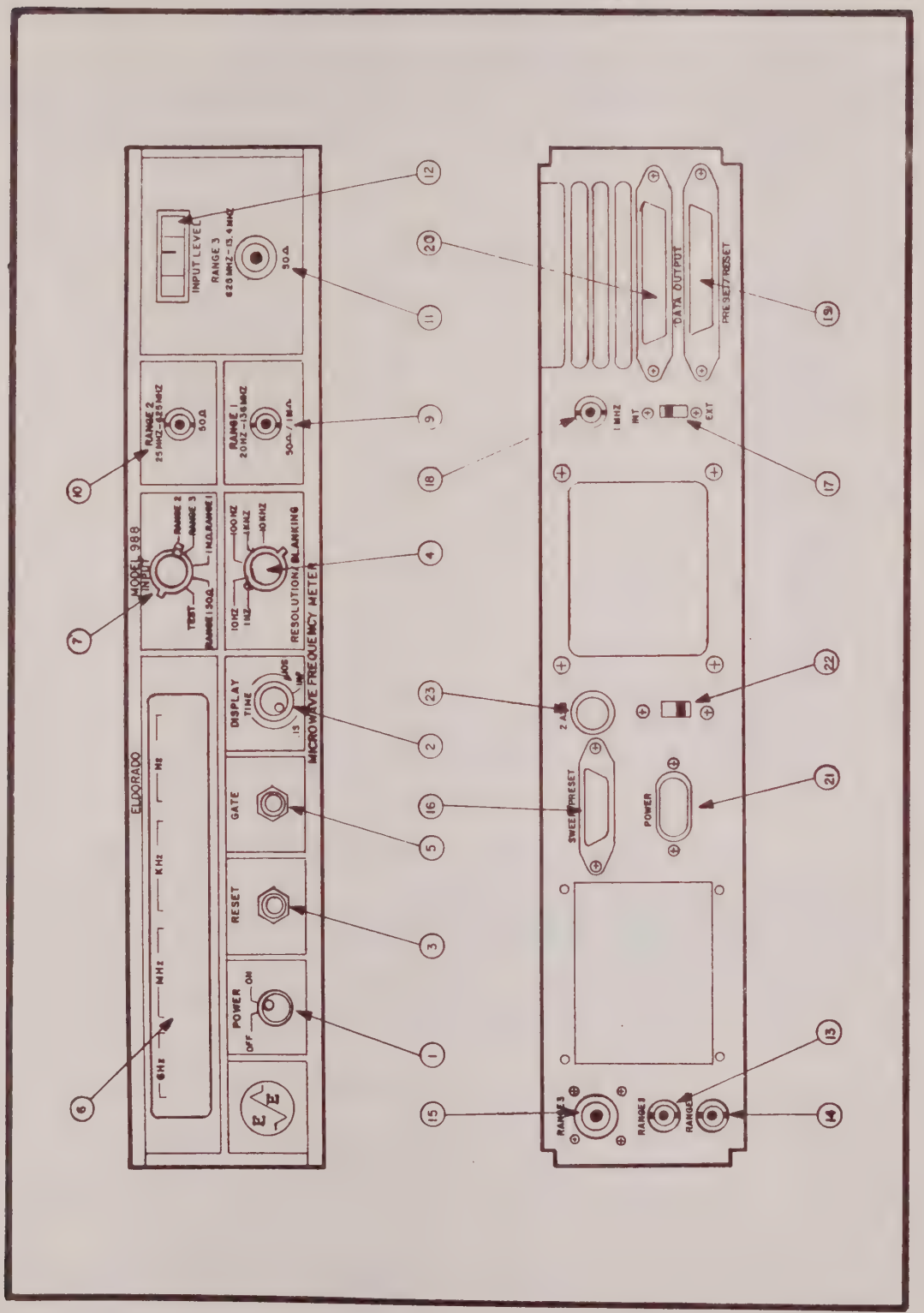


FIGURE 2-1

FRONT AND REAR PANEL CONTROLS, INDICATORS AND CONNECTORS

TABLE 2-3

DIGITAL DATA CONNECTOR WIRING OPTION P

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	10^0 1 bit	26	10^0 4 bit
2	10^0 2 bit	27	10^0 8 bit
3	10^1 1 bit	28	10^1 4 bit
4	10^1 2 bit	29	10^1 8 bit
5	10^2 1 bit	30	10^2 4 bit
6	10^2 2 bit	31	10^2 8 bit
7	10^3 1 bit	32	10^3 4 bit
8	10^3 2 bit	33	10^3 8 bit
9	10^4 1 bit	34	10^4 4 bit
10	10^4 2 bit	35	10^4 8 bit
11	10^5 1 bit	36	10^5 4 bit
12	10^5 2 bit	37	10^5 8 bit
13	10^6 1 bit	38	10^6 4 bit
14	10^6 2 bit	39	10^6 8 bit
15	10^7 1 bit	40	10^7 4 bit
16	10^7 2 bit	41	10^7 8 bit
17	10^8 1 bit	42	10^8 4 bit
18	10^8 2 bit	43	10^8 8 bit
19	10^9 1 bit	44	10^9 4 bit
20	10^9 2 bit	45	10^9 8 bit
21	10^{10} 1 bit	46	N/C
22	Positive Inhibit $\geq$ 2 to 5V	47	Neg. Inhibit to 0V
23	Pos. Print Command, 0 to 5V	48	N/C
24	0V (low reference; ground)	49	N/C
25	+5V (high reference)	50	Ground

NOTES:

1. 10^0 is the least significant digit printed out and is the Units of Hertz column.
2. The Reference Voltage is obtained from a voltage divider comprised of a 1k to +5volt network and is referenced to a -12V or +12V source. The reference voltage output at pin 25 is $\simeq$ 5V.
3. Binary Data. 1-2-4-8 BCD; positive zone positive true, binary "0" = 0V, binary "1" = +5V.
4. (+) Print Command: Positive going step at the end of the count cycle from 0V to 5V nominal.
5. Output connector is an Amphenol 57-40500. Mating connector is Amphenol 57-30500.

TABLE 2-4

REMOTE PROGRAM OPTION J

REMOTE PRESET/OFFSET OPTION F

CONNECTION WIRING

PIN NO.		FUNCTION	PIN NO.		FUNCTION
1	Option F	10^3 1 bit	26	Option F	10^3 4 bit
2		10^3 2 bit	27		10^3 8 bit
3		10^4 1 bit	28		10^4 4 bit
4		10^4 2 bit	29		10^4 8 bit
5		10^5 1 bit	30		10^5 4 bit
6		10^5 2 bit	31		10^5 8 bit
7		10^6 1 bit	32		10^6 4 bit
8		10^6 2 bit	33		10^6 8 bit
9		10^7 1 bit	34		10^7 4 bit
10		10^7 2 bit	35		10^7 8 bit
11		10^8 1 bit	36		10^8 4 bit
12		10^8 2 bit	37		10^8 8 bit
13		10^9 1 bit	38		10^9 4 bit
14		10^9 2 bit	39		10^9 8 bit
15		10^{10} 1 bit	40		10^{10} 8 bit
16	Option J	TEST	41		N/C
17		Range 1	42		N/C
18		Range 2	43		N/C
19		Range 3	44		N/C
20		RESET	45		N/C
21		Display Time	46		N/C
22		Display Time Rtn.	47	Option F	Preset Enable
23		N/C	48		N/C
24		oV (Low Reference: Ground)	49		N/C
25	Option F	+5V (High Reference)	50		Ground

NOTES: Option F Remote Preset/Offset.

1. 10^3 is the least significant digit to be preset and is the 1 kHz column. All decades through to 10^9 can be preset to any number from 0 to 9.

2. 10^{10} is the most significant digit to be preset and is the 10 GHz column. This decade can only be preset to 0, 1, 8 or 9.

NOTES: Option J Remote Program.

1. Ground applied to any of the respective pins will provide remote control of the portion of the counter.

2. Display Time (pin 21) and Display Time Ground (pin 22). An external 1 MΩ (max.) between pin 21 and 22 will provide display time control.

SECTION 3

THEORY OF OPERATION

SECTION 3
THEORY OF OPERATION

3.1 GENERAL

This section describes the Model 988/989 Microwave Frequency Counter on a functional diagram level.

The Model 988/989 is designed to perform frequency measurements, on three bands, from 20 Hz to 18 GHz automatically. The instrument employs three basic frequency measurement techniques to accomplish such a wide frequency coverage. Frequencies from 20 Hz to 136 MHz are measured using conventional direct counter techniques, i.e., the input signal is applied directly to a count chain which has a gate controlled by a precision time base counter. Frequencies from 25 MHz to 625 MHz utilizes pre-scaler techniques. to count down (divide) by four the input frequency before applying it to the count chain for direct counting. Frequencies from 0.6 GHz to 18 GHz are measured using both the heterodyne and direct counting technique, i.e. the input signal is first scaled down via heterodyning to an IF convertion frequency and then direct counted. The direct counter is first preset (the three most significant digits) and then allowed to count the output from the automatic heterodyne converter. Thus the direct counter frequency range is expanded to 18 GHz. Frequencies to 13.4 GHz are made on the Model 988 with frequency measurements to 18 GHz on the Model 989. Basic circuit operation is identical for both instruments with slightly different frequency determining components employed to cover the different frequency bands.

Operation on any range is by the simple task of connecting the input signal to one of three input connectors and selecting the desired input by switch action. Frequency measurements are thereafter made continuously, at rates from ten per second to one per four seconds, providing a direct reading 11 digit display. No interpolating, fine tuning or outside mathematics are necessary by the operator.

The visual display is presented on eleven in-line digital display indicators sectionalized so that the unit of measurement is immediately apparent. Store display feature is provided with updating, once per measurement period. Display time independent of gate time is variable from 0.1 seconds to ten seconds with a switch selected infinite hold position incorporated into the control. Reset is automatic and is produced at the end of the display period. In the infinite display setting automatic reset is not produced and manual reset is required by front panel switch action or remotely via a rear panel connector when optioned. Time base selection and blanking in five steps provide the operator a choice of resolution from 1 Hz to 10 kHz.

3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS

Figure 3-1 illustrates the Model 988/989 as divided into functional operational sections and subsections. The two main sections are the Automatic Heterodyne (Auto Het)/Input Section (A1 and the Counter/Display Section (A2).

The Auto Het/Input Section (A1) is physically located on a single chassis assembly and consists of seven plug-in P.C. boards which comprises an operational subsection that provides for the signal input processing and Auto Het control. Located on this same chassis are the components that make up the RF subsection. Listed below in Table 3-1 are the assemblies with their reference designator and drawing control numbers or part numbers.

TABLE 3-1

AUTO HET/INPUT SECTION (A1) ASSEMBLIES

Ref. Designator	Name	Part No./Dwg. Cont. No
A1A1	Range 1 and 2 Input Amplifier P C B Assembly	32-10731
A2A1	Input Control and 1st DCU	32-10865
A1A3	Sweep Generator P C B Assembly	32-10729
A1A4	Start Detector P C B Assembly	32-10728
A1A5	Digital-to-Analog Converter P C B Assembly	32-10727
A1A6	YIG Driver/Controller P C B Assembly	32-10726
A1A7	Stop Detector P C B Assembly	32-10724
A1A8	YIG Tuned Multioctave Multiplier	95-10047
A1A9	200 MHz Power Amplifier Assembly	34-09571
A1A10	Low Pass Filter Assembly	95-10126
A1A11	200 MHz Frequency Multiplier Assembly	34-09572
A1A12	20 MHz Phase Lock Oscillator Assembly	34-10733
A1A13	I. F. Amplifier Assembly	34-10734
A1A14	Hybrid Coupler Assembly	CL-A19
A1A15	Back Diode Detector	DA-12
A1A16	"Auto Het" Mother Board	33-10723

The Counter and Display Section is located on a seperate P C B Assembly (A2) and is assigned a part number of 33-09622. The Display Subassemblies (A2V1 thru A2V11) which provides the 11 digit visual display are assigned the part number 33-10719.

The subsections that make up the Counter and Display Section are listed in Table 3-2 by their functional name and the schematic and figure number of the schematic located in section 6 of this manual.

TABLE 3-2

COUNTER AND DISPLAY SECTION FUNCTIONAL SUBSECTIONS

Functional Name	Schematic Dwg. No.	Figure No.
Time Base	D-11-09585	6-1
Control Logic	D-11-09582	6-3
Count Chain	D-11-09587	6-4
Strobed Display Logic	D-11-10123	6-5
Display Logic and Visual Display	D-11-10123	6-5

The instruments power supply (A3) is physically located on a seperate P C B and utilizes integrated circuits for regulation (A3U2 thru A3U7). Power transformers which are rear panel mounted supply the required ac voltages to the A3 P.C. board. Transformer T1 is the main power transformer and has one -2 terminal output for the 190 volt dc rectifier and three center taped secondaries for the +18 volt, the +12 and -12 volt, and the +5 and -5 volt regulated supplies. When E option is included within the instrument transformer T2 is added to provide voltage for the optioned regulated +28 volt supply components located on the PCB.

3.2.1 RANGE 1 FUNCTIONAL OPERATION

When the instrument is placed in Range 1 (20 Hz to 136 MHz) operation direct counting technique is used and the following functional assemblies/subassemblies (see Figure 3-1) are utilized.

Front panel controls (A4)
Range 1 circuitry of A1A1 PCB
Input Processor PCB (A1A2)
Counter PCB (A2)

The signal to be counted is applied to the front panel RANGE 1 input connector and coupled via a coax cable to PCB assembly A1A1J1, and the front panel INPUT switch is placed on the RANGE 1-50Ω or the Range 1 - 1 MΩ position. If the INPUT switch has been placed in RANGE 1-50Ω position the $\overline{\text{RANGE 1 50Ω ENABLE}}$ signal is set at "0" state (ground) level and a relay (A1A1K1) located on the A1A1 PCB will effect a shunt of the range 1 input FET amplifier with a 50Ω resistor. When the INPUT switch is placed in the RANGE 1-1MΩ position (or RANGE 2 or RANGE 3 position) the input impedance select relay (A1A1K1) will de-energize and the range 1 input will exhibit a 1MΩ input

impedance. The range 1 input signal is amplified by a FET input amplifier and ECL logic wide band amplifiers and outputed at A1A1J2 to the Input Processor PCB assembly A1A2J3 input connector.

The Input Processor performs gate selection by ECL logic when the RANGE 1 ENABLE signal is placed low (ground) by INPUT switch action. The gate selected range 1 signal is then applied to a BCD counter (1st DCU) and outputted as a 1-2-4-8 BCD signal via ECL-to-TTL translators to the counter PCB assembly (A2) after count gate on time. The first DCU and BCD ECL-to-TTL translators are enabled when the GATE signal from A2 PCB control logic is at its high ("1") state.

The Counter PCB assembly A2 contains the count chain, strobe display logic, time base logic and control logic.

The count chain and strobe display logic circuits perform the following: Counting of the inputed BCD signal from the first DCU located on the A1A2 PCB assembly, storage of the counted data and its conversion to decimal data for display on the 11 digit strobed display assembly (A2A1).

The time base and the strobed display logic circuits interfaces with the front panel RESOLUTION/BLANKING switch which selects resolutions of 1 Hz, 10 Hz, 100 Hz, 1 kHz or 10 kHz and provides the blanking of the least significant digits so the display will relate to the resolution selected.

Gate times generated when range 1 (or range 3) operation is selected, is 1 second for 1 Hz resolution and 0.1 second for 10 Hz thru 10 kHz resolutions. Gate time is determined by the $\overline{\text{CLOCK}}$ signal which is generated by the time base logic circuits by counting down the 1 MHz reference clock (TB CLOCK signal).

The control logic circuits receive the $\overline{\text{CLOCK}}$ signal from the time base logic and interfaces with the front panel DISPLAY TIME control and generates the GATE, STORE, RESET, PRESET ENABLE, and PRINT COMMAND signals.

3.2.2 RANGE 2 FUNCTIONAL OPERATION Range 2 (25 MHz to 625 MHz) operation makes use of the prescalling ($\div 4$) followed by direct counting technique. When the instrument is operated in range 2 the following assemblies, subassemblies and circuits (see Figure 3-1) are used.

Range 2 input amplifier and prescaler circuit located on subassembly A1A1.

Input Processor subassembly A1A2.

Counter PCB assembly A2.

The signal to be counted is applied to the RANGE 2 front panel connector (A4J2) and the INPUT switch (A4S2) is set to the Range 2 position. The signal input is coax cabled to A1A1J3 and applied to a two stage common-emitter RF amplifier circuit utilizing special NPN silicon low noise RF transistors. After being amplified and conditioned to a -5.2 volt ECL compatible digital signal it is prescaled (divided by four) by a ECL counter circuit and outputted to the Input Processor via output connector A1A1J4.

The Input Processor (A1A2) performs gate selection of the prescaled range 2 signal by ECL logic when the $\overline{\text{RANGE 2 ENABLE}}$ signal is placed low by the INPUT switch. The signal is converted to a 1-2-4-8 BCD signal and then applied to the Counter PCB assembly (A2). The first DCU and counter functions are the same in operation as the range 1 direct counting functions as previously described in paragraph 3.2.1 of this section except for the time base selection.

The $\overline{\text{RANGE 2 ENABLE}}$ signal (identified as $\overline{\text{PRESCALE}}$ on the time base logic schematic will cause the time base ($\overline{\text{CLOCK}}$) gate to be increased by a factor of four in gate length thus providing a $\overline{\text{GATE}}$ signal of 4 seconds when 1 Hz is selected and 0.4 seconds when 10 Hz through 10 kHz is selected by the

RESOLUTION/BLANKING switch (A4S3).

3.2.3 RANGE 3 FUNCTIONAL OPERATION When the instrument is placed in range 3 operation (0.6 GHz to 13.4 GHz for the Model 988 and up to 18 GHz for the Model 989) the automatic heterodyne measurement technique is used. All assemblies, subassemblies and logic circuits of the Model 988/989 are utilized when counting in the range 3 configuration, other than the Input Amplifier Prescaler subassembly (A1A1) (refer to Figure 3-1 for the functional interconnect and control and logic interface).

The accuracy of the range 3 measurements are related to the 1 MHz crystal controlled reference oscillator (A7) in two ways. The generation of the time base (length of the $\overline{\text{CLOCK}}$ signal) by counting down the TB CLOCK signal is one of the 1 MHz reference oscillator related functions (this function is also utilized in range 1 and 2 operation). The other 1 MHz clock related function is the generation of the 200 MHz YIG drive which is referenced to the 1 MHz clock. This frequency multiplication of 1 MHz to 20 MHz is accomplished using digital phase-lock techniques for multiplication to 20 MHz, and RF multiplication techniques from 20 MHz to 200 MHz.

The subassemblies that perform the 200 MHz YIG drive generation are the 20 MHz Phase Lock Oscillator (A1A12), the 200 MHz Frequency Multiplier (A1A11) and the 200 MHz Power Amplifier (A1A9). The CLOCK signal is outputted from the Clock Control PCB assembly (A6) and applied to the 20 MHz Phase Lock Oscillator.

The Phase Lock Oscillator assembly (A1A12) consists of a 20 MHz voltage controlled oscillator (VCO) circuit which is controlled (phased locked) by a IC phase-frequency detector circuit type MC4044. Functionally this device monitors the 1 MHz inputted CLOCK signal and the 20 MHz VCO output which is counted down to 1 MHz by a DCU and generates a correction voltage when any difference in phase is noted, this correction voltage changes the frequency of the VCO to maintain a frequency lock-on condition thus performing the function of a phase lock loop.

The 200 MHz Frequency Multiplier (A1A11) multiplies the 20 MHz sinewave from the 20 MHz Phase Lock Oscillator to 200 MHz by the use of tuned RF amplifiers tuned to the 2nd and 5th harmonics thus providing a X 10 overall frequency multiplication factor. The multipliers output is applied to the 200 MHz Power Amplifier subassembly (A1A9).

Assembly A1A9 the Power Amplifier consists of three RF NPN transistor amplifiers tuned to 200 MHz. The collector voltage applied to the 2nd and 3rd amplifiers is adjustable by a chassis mounted Power Level Control (A1R2) which determines the amount of drive to the YIG (0.5 to 1.0 watts nominal).

To explain the Model 988/989 auto-heterodyne conversion we will have to relate to a signal of a certain frequency that is to be measured, so lets assume that an input signal of 13,051,200,000 Hz (13.051200000 GHz) is applied to the range 3 input connector. From the range 3 front panel connector the input signal is coax cabled to the Hybrid Coupler (A1A14) which has a band pass of 18 GHz and low insertion loss from 0.6 to 18 GHz thus allowing range 3 signals to be inserted and passed to the BACK DIODE DETECTOR (A1A15). Upon the presence of an input signal the BACK DIODE DETECTOR will generate a dc level which is relative to the input signals amplitude, this signal is called out in Figure 3-1 as the DET CURRENT signal. The DET CURRENT signal is amplified by a differential amplifier located in the input of the Start Det logic which is part of subassembly A1A4, and is used to drive the front panel RANGE 3 INPUT LEVEL METER (A4M1) and the Start Dectector logic. The Start Detector logic generates

a START signal when the amplified detector current reaches an adjustable threshold set by the START LEVEL control located on PCB subassembly A1A4, this START signal is gate enabled when the RANGE 3 ENABLE signal is set low by the front panel INPUT switch. The START signal is applied to the Sweep Generator (A1A3) and gates on a free-running 50 kHz M.V. which clocks the sweep generation logic. Sweep generation logic outputs a BCD formatted DIGITAL SWEEP (BCD) signal to the D/A converter subassembly (A1A5).

The D/A Converter (A1A5) translates the BCD sweep into an analog step ramp which in turn is amplified by the YIG Driver and Leveler subassembly (A1A6). This analog ramp is applied to the YIG coil drive transistor (A1Q1) which produces an ever increasing magnetic flux across the YIG causing the YIG to scan through its comb lines. The relationship between the magnetic flux and the comb line frequency is 2.8 MHz/oersted or can be stated in drive current as 17-22 MHz/ma.

When the 13.0 GHz comb line is reached an intermediate frequency (IF) of 51.2 MHz is generated by the heterodyning of the 13.0512GHz inputted signal and the 13.0 GHz YIG outputted (comb line), by the Back Diode detector (A1A15).

The 51.2 MHz IF signal is amplified by the IF amplifier assembly (A1A13) and applied to the Stop Det and IF Shaper assembly (A1A7) as the HET IF SIGNAL. The Stop Detector logic generates a STOP signal on the presence of an IF signal, which is outputted to the Sweep Generator assembly (A1A3) and the Start Det and "N" Preset assembly (A1A4). The STOP signal that is routed to the Sweep Generator assembly terminates (stops) the DIGITAL SWEEP (BCD) count thus locking the heterodyne converter to the input signal. At the same moment the STOP signal signals the "N" preset count logic located in assembly A1A4 that lock-on has been achieved and outputs the preset count of 130 which is preset into the Count Chain located in assembly A2.

The 51.2 MHz IF signal is shaped and converted to a ECL compatible logic level by common emitter coupled amplifiers which constitute the IF shaper circuits of assembly A1A7 and outputs the shaped IF signal to assembly A1A2 via connector A1A7J2.

The shaped 51.2 MHz IF signal applied to A1A2J2 is gate selected when the RANGE 3 ENABLE is set low by the setting of the INPUT switch in the RANGE 3 position and applied to the first DCU. The first DCU counts the 51.2 MHz signal for a period of 100 ms which is the period of the GATE signal which is inverted to provide an enable for the first DCU. The first DCU outputs its count in 1-2-4-8 BCD format to the Count Chain located on PCB assembly A2 as TTL compatible +5V logic where it is added to the preset "N" count of 130 thus providing a direct counter reading of 13,051,200,000. This counter reading is converted to decimal form by the Strobe Display Logic and the 11 Digit Strobe Display assembly will display the counter reading directly as 13,051,200,000 which is the measurement readout of the range 3 input signal.

As long as the range 3 input signal is present and of a level of 100 mv rms or greater the heterodyne converter will remain in a lock-on state, sample and provide readouts at a 4 times per second rate. When the range 3 input signal is removed, decrease to a level of less than 100 mv rms or its frequency is changed so that the resultant IF frequency exceeds the band width of the IF amplifier the hetrodyne converter lock-on will be dropped and the auto converter will enter a ready state until another input signal is intercepted (generation of a START) thus locking on and entering a count state.

The sweep search rate is about 50 ms per GHz or 230 ms minimum to about 0.9 seconds maximum.

3.2.4 POWER SUPPLY AND POWER DISTRIBUTION FUNCTIONAL ANALYSIS

The ac 115 volt 60 Hz single phase line source power is applied to a rear panel mounted three pin Connector/Line Filter assembly (A5FL1)/J4) its ground conductor is connected at a rear panel common ground point. The ac neutral is distributed to neutral connections of the Power Transformer (A5T1), the Fan Motor (A5B1) and the internal heater element of the 1 MHz Reference Oscillator (A7). The hot side of the ac is applied to a 2 amp S.B. Fuse (A5F1) and then wired to the hot side of the Reference Oscillator's internal heater element thus allowing the Reference Oscillator oven to remain operational when the instrument is plugged into the line source regardless of the setting of the front panel POWER OFF/ON switch. The load side of the ac line fuse is also wired to the line side of the front panel ON/OFF switch (A4S1) and in turn the load side of the switch is wired to the Fan Motor (A5B1) and the Power Transformer (A5T1) allowing the switching of the instruments Power Supply and Fan Motor on or off from the front panel.

The secondary windings of the Power Transformer (A5T1) is hard wired to the Power Supply assembly (A3). This Power Supply assembly contains the diode rectifiers, IC Voltage Regulators and RC Filter components for the development of the required dc output voltages. Table 3-3 lists the dc voltages, their function and the PCB A3 pad numbers of the output voltage connections.

TABLE 3-3

POWER SUPPLY (A3) OUTPUT VOLTAGES

OUTPUT	FUNCTION	A3 PAD NO. (S)
+190 V unregulated	Display Tube Anodes	3
+190 V ground return		4
+28 V unregulated	YIG Oven Heater	1
+28 V ground return		2
+18 V regulated	YIG Tuning Coil	13
+18 V ground return		12
+12 V regulated	Amplifier V_{cc}	9 & 10
-12 V regulated	Amplifier Vee	5
±12 V ground return		6, 7, & 8
+5.0 V unregulated	Clock Control A5A1	U
+5.0 V ground return		T
+5.0 V regulated	Auto Het V_{cc}	11
+5.0 V regulated	Counter V_{cc}	20 & 21
-5.0 V regulated	Auto Het V_{cc}	18 & 19
±5.0 V ground return		14, 15, 16 & 17

The dc voltages applied to the auto het plug in PCB assemblies A1A1 thru A1A7 are distributed via the Auto Het Mother PCB A1A16 being hard wired from the Power Supply assembly A3 to the Auto Het Mother Board A1A16 then distributed via the PCB traces to the PCB connectors (refer to the individual PCB assembly schematic diagrams in Section 6 of this manual for pinning information of the applied dc voltages.

The PCB assemblies A1A9, A1A11, A1A12 and A1A13 located in the auto het RF section (Chassis mounted) are enclosed in RF shield subassemblies and receive their dc voltages via feed thru capacitors and ferrite bead filters thus allowing filtering of the dc voltages as well as maintaining the integrity of the RF shielding.

3.2.5 INPUT/OUTPUT OPTIONAL INTERFACE FUNCTIONAL ANALYSIS

When options F, P or S are installed rear panel mounted multi pin Amphenol 57-40000 series connectors are provided. Figure 3-1 calls out the connectors and indicates the optional functional interfaces.

Option F provides a remote preset and offset BCD input to the count chain logic via connector A5J2 by 30 lines of BCD coded inputs of isolated contact closures to ground or saturated NPN transistors to ground (TTL logic). This option allows presetting the count chain to any desired count from all zeros to 19999999000 in increments of 1kHz. This function provides for local oscillator monitoring of a unit under test or similar applications where an offset of the display count is required.

Option P interface is a measurement data output in BCD 1-2-4-8, 11 digit format (44 lines) from the count chain via an extender PCB/connector assembly to the rear panel. A PRINT COMMAND and ± INHIBIT signals are also provided which interface with the control logic by hard wiring. The connector is a 50 pin Ampheno 57-40500 and is referenced as A5J1. This output data is positive zone true logic "1" = 5V and "0" = 0V.

Option S interface is provided by connector A5J3 which is hard wired to the Sweep Generator PCB A1A3, this optional interface consist of 18 lines BCD in the following format.

10^0 bits 2-4-8
10^1 bits 1-2-4-8
10^2 bits 1-2

and provides selection of the three MSD of start frequency (lowest frequency) and stop frequency (highest frequency) that the range 3 function will sweep.

3.3 DETAILED THEORY OF OPERATION

This subsection describes the circuitry of the Model 988/989 Microwave Frequency Counter at the logic and circuit level, in considerable detail. The figure number in parenthesis, when included with the paragraph title heading, refers to the circuit schematic located in Section 6 of this manual. Integrated circuits (IC's) which are incorporated into this instrument are detailed by integrated circuit data sheets located in Section 6 of this manual and provide the following information.

1. Pinning data and device outlines.
2. Circuit schematic equivalents.
3. Logic diagrams.
4. Truth tables when required.
5. Description of the device as to logic function and application.

In the cases of the YIG Tuned Multioctave Multiplier (A1A8), the Low Pass Filter (A1A10), the Hybred "T" (A1A14) and the Back Diode Detector (A1A15) the detailed theory of operation is not circuit or logic related because these devices contain no circuits as such, and are described as to the physical and or RF principals involved.

3.3.1 YIG TUNED MULTIOCTAVE MULTIPLIER ASSEMBLY A1A8

The heart of the Multioctave Multiplier is the Yttrium-Iron-Garnet (YIG) which is a synthetically grown tri-valence crystal of yttrium and iron oxide. When it is processed into a high tolerance polished sphere it exhibits a high Q ferromagnetic resonance at which the apparent permeability of the yttrium oxide reaches a sharp maximum. This resonance occurs in the presence of a steady state transverse magnetic field when the microwave frequency equals the precession frequency of the electron orbits of the yttrium atoms. The resonance frequency depends solely on the flux of the transverse magnetic field. The resonant frequency is equated as $F_0 = vH$, where H is the magnetic field strength in oersteds (1 ampere-turn/inch = 0.495 oersted), and v is a constant (2.8 MHz/oersted) which is the frequency/magnetic field relationship of the YIG. The significance of this equated statement is that the resonant frequency (F_0) depends only on the flux of the applied magnetic field and not on the diameter or any other physical aspect of the YIG sphere. The degree of spherical accuracy (run-out) is the Q determining factor of the resonant system and in this case is specified as adjacent harmonic and unwanted signal rejection as referenced to the leveled selected harmonic output as being -60 db or greater.

The YIG tuned multioctave multiplier assembly (A1A8) is contained in a 2 x 2 x 2.8 inch RF and magnetic shielded enclosure weighing 29 ounces and contains the YIG, a 100 mH tuning coil, an internal heater element, input and output RF connectors, and terminals for applying the coil drive, diode bias and heater current connections.

No adjustments are provided or required for the YIG operation because the development and calibration of the coil drive current and leveling signal (diode bias) is provided for by the YIG Driver and Leveler PCB assembly (A1A6). For the purpose of instrument maintenance the YIG assembly can be treated as a "Black Box" having an input and output port and control signals applied. The following table of specifications is provided to aid the technican in determining if the YIG assembly is functioning correctly and if the interfacing of the coil drive current, diode bias, and 200 MHz drive is correct.

TABLE 3-4

YIG TUNED MULTIOCTAVE MULTIPLIER SPECIFICATIONS

Input Frequency	200 MHz
Input Power Level	.5W - 1.0W
Input Impedance @ 1W	50 Ohm
Input VSWR @ 1W	2:1 (typical)
Output Frequency	.6 - 13.4 GHz and .6 - 18.0 GHz
Output Power Level	See Figure 3-2
Adjacent harmonic rejection and unwanted signal rejection	Adjacent harmonic rejection and unwanted signal rejection referenced to the leveled selected harmonic power output, 60 db down, minimum
200 MHz Direct Feedthrough	-50 dbm maximum
Maximum frequency Drift (+10°C to +65°C) (measured into 50 Ohm load)	35 MHz maximum
Linearity Error	± 18 MHz maximum
Tuning Sensitivity	(typical) 17 - 22 MHz/ma
Tuning Coil Resistance	10 Ohm maximum
Tuning Coil Inductance	(typical) 100mH
Repeatability (up from zero current)	.15% minimum
Heater Current @ 22 - 30 VDC	1.0A maximum Surge @ 10°C .2A maximum continuous
Output Leveling: The comb output power, including the effect of spurs and ripple, is within the limits specified in Figure 3-2. Power output of adjacent comb lines do not vary by more than 5 db.	
Spurs and ripple in pass band and filter skirts (in leveled condition)	3 db
Temperature Range	
Size (excluding connectors)	2 x 2 x 2.8 inches (maximum)
Weight	29 Ounces (maximum)

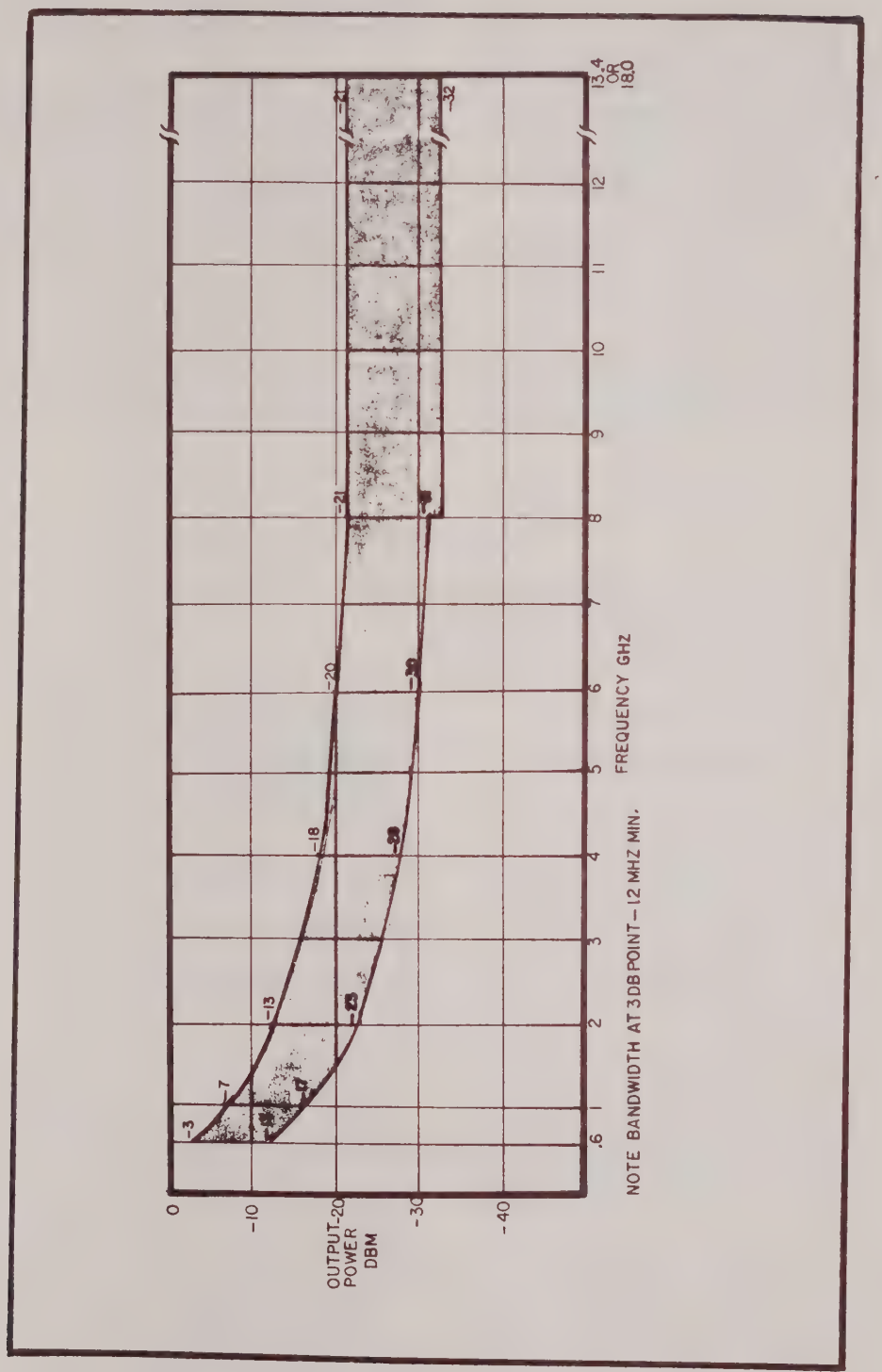


FIGURE 3-2
YIG POWER OUTPUT/FREQUENCY

3.3.2 LOW PASS FILTER ASSEMBLY A1A10

The Low Pass Filter is contained in a 2.0 inch long by 0.375 inch diameter assembly with SMA 3 millimeter male input connector and female output connector, having 50 ohms input/output impedance. The Filter Assembly is inserted between the Hybrid Coupler (A1A14) and the Back Diode Detector (A1A15), when required to maintain spectral purity (not all Model 988/989A Counters require this filter). The filter's band pass is dc-to-18 GHz with an insertion loss of no greater than 0.75 db and a VSWR specification of 1.7: 1 maximum. High band rejection is 35 db minimum from 21.5 GHz to 24 GHz. The sole function of the filter assembly is to reject harmonics above 18 GHz from being inserted into the Back Diode Detector.

3.3.3 HYBRID COUPLER ASSEMBLY A1A14

The Hybrid "T" is a multioctave 90^0 quadrature phase hybrid (crossover) network utilizing strip-line techniques. Basically its a 3 port "black box" directional coupler with a frequency range of 7.0 GHz to 18.0 GHz. The inputs are the range 3 625 MHz to 18 GHz input signal and the YIG tuned multioctave multiplier's output via the low pass filter. Its output is applied to the back diode detector assembly (A1A15). The complete specifications for this device is provided in Table 3-5.

TABLE 3-5

HYBRID COUPLER ASSEMBLY A1A14 SPECIFICATIONS

Frequency Range:	7.0 GHz to 18.0 GHz
Frequency Sensitivity:	±0.5 db Maximum
VSWR:	1.35 : 1 Maximum
Impedance:	50Ω
Coupling:	3.0 db (+0.3 - 0 db)
Isolation:	15 db Minimum
RF Input Power:	50 Watts CW Maximum
Weight:	0.9 Ounces
Connectors:	SMA 3 mm male coax

3.3.4 BACK DIODE DETECTOR ASSEMBLY A1A15

The back diode detector assembly is a tunnel diode detector mounted in a Aerteck Industries® Do series mount, part number DO218B. This device provides broad band, flat response, and high sensitivity with a very low dynamic resistance. The input (RF) port is a SMA 3 millimeter male connector, and the output (video port is provided for by a SMA 3 millimeter female connector. The mount has a total length of 2.125 inches and a body diameter of 0.3125 inches. Table 3-5 provides the basic device specifications.

TABLE 3-5

BACK DIODE ASSEMBLY SPECIFICATIONS

Input Capacitance:	15 pFd Maximum
Open Circuit Voltage Sensitivity (K):	400 mv/mw Minimum
Figure of Merit (M) where $M = \frac{K}{\sqrt{R_V}}$:	40 minimum
VSWR:	4 : 1 Maximum 3 : 1 Typical
Flatness (the RF power variation required to maintain a constant voltage output over the frequency range):	± 1 db Typical
Maximum Input Power:	10 milli Watts CW 1 erg Spike
Maximum Forward Voltage:	0.5 Volts
Maximum Reverse Current:	10 mA

When performing test and or alignment procedures insure that the above voltage and power specifications are not exceeded or permanent damage to the detector may result. During normal operation of the instrument insure that the range 3 input signal is less than 2.2 volts rms (+20 dbm) to prevent burn out of the detector. Generally a tunnel diode's power handling capabilities are much higher than that of point - contact detector crystals; however, because of the low video resistance (R_V) being in the order of 100 ohms as compared to 5k ohms it is much easier to exceed power ratings through transient voltages spikes.

3.3.5 20 MHz PHASE LOCK OSCILLATOR ASSEMBLY A1A12 (Figure 6-15)

The 20 MHz phase lock oscillator provides a stabilized 20 MHz sinewave output which is referenced to the 1 MHz internal crystal

oscillator located in assembly A7 that has a stability of 7 x 10^{-9} per day. Or can be referenced to an external oscillator source when the rear panel EXT/INT switch is placed in the EXTernal position.

The circuitry that comprise the 20 MHz phase lock oscillator consist of a 20 MHz crystal voltage controlled oscillator (VCO) a digital divide-by-twenty control loop and a digital phase comparator frequency detector. Figure 6-15(C-11-09450) provides the schematic diagram for the assembly and the following description relates to this schematic.

The VCO is a free running 20 MHz crystal oscillator comprised of Q1, Y1, CR1, C5 and associated circuitry. Crystal Y1 provides the initial frequency control and CR1 functions as the fine tuning voltage controlled varicap which causes the output to be phase locked to the 1 MHz reference. The variable capacitor C5 provides a course alignment adjustment of the oscillator and is adjusted for +8 volts at the test point (T.P.) Transistor Q2 and its associated circuitry comprises a 20 MHz amplifier driver which outputs the 20 MHz sinewave to the assembly output coax connector. Transistor Q3 and its associated components function as a 20 MHz amplifier buffer and outputs to the digital divide-by-twenty control loop.

The divide-by-twenty control loop is configured by IC modules U3B and U2. U3B IC element is a J-K flip flop which is toggled by the 20 MHz sinewave signal and functions as a divide-by-two binary, outputting a 10 MHz digital signal at the Q output pin 9. This 10 MHz signal is applied to U2 pin 1. U2 is a type 7490 IC decade counter that is configured as a symmetrical divide-by-ten counter by connecting its A input at pin 14 to the D output (pin 11) and taking the ÷ 10 square wave output at A OUT (pin 12), this output which is a symmetrical 1 MHz digital signal is applied to the V_1 input of the phase detector IC (U1 pin 3).

The phase comparator frequency detector is an IC circuit type MC4044 (U1). This IC device contains two digital detectors and a charge pump circuit which converts the +5 volt digital 1 MHz inputs to a dc voltage level for use in controlling the frequency of the 20 MHz VCO. The two phase detectors (see Figure 3-3 Frequency Detector Functional Block Diagram) have common inputs. Phase frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (V1) and reference input (R1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty of cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles.

The charge pump accepts the phase detector outputs (U1 or U2) applied to PU and D1 or D2 applied to PD and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4044 circuit. The filter provides a dc voltage proportional to the phase error.

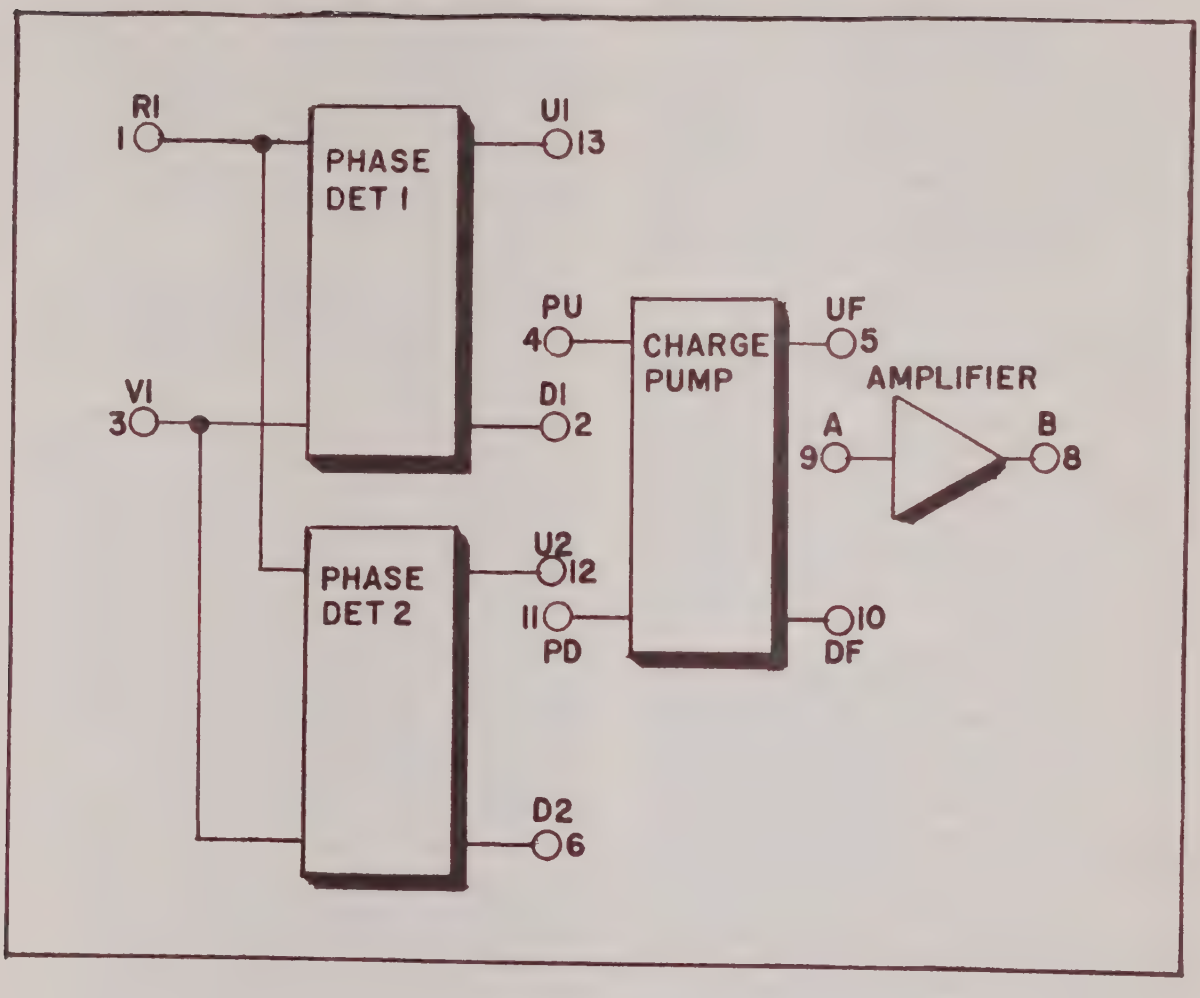


FIGURE 3-3
MC4044 FREQUENCY DETECTOR FUNCTIONAL BLOCK DIAGRAM

3.3.6 200 MHz FREQUENCY MULTIPLIER ASSEMBLY A1A11 (FIGURE 6-14)

The 200 MHz frequency multiplier provides for the multiplication of the 20 MHz sinewave from the phase locked oscillator assembly A1A12 to 200 MHz. The following detailed analysis is referenced to Figure 6-14 200 MHz Frequency Multiplier Schematic (C-11-09469).

All the components except the "feed thru" capacitor C21 are mounted on a PCB which is enclosed in an RF shielded cover assembly. The +12 volt V_{CC} is applied via the "feed thru" capacitor C21 and inductor L4 which is actually the V_{CC} lead fed through two ferrite beads. This configuration allows the insertion of the V_{CC} voltage while maintaining the integrity of the RF shielding and provides low pass filtering.

The input 20 MHz sinewave signal is applied to the input coax connector and is coupled to the base of transistor Q1 via a network consisting of R1, C1, C2 and L1. Resistor R1 sets the input impedance at 50 ohms and the LC component form a resonant 20 MHz tuned input coupling circuit. The collector circuit of transistor Q1 is tuned to the fifth harmonic of the 20 MHz input (100 MHz) by the tank circuit comprised of L5, C3, C4 and C20. A coupling network consisting of L6, L7, and C7 thru C10 couples the 100 MHz signal to the base of transistor Q2. The collector circuit of transistor Q2 is tuned to 200 MHz and coupled to the base of transistor Q3 by the LC lumped and distributed circuit elements. Transistor Q3 provides the output drive via its tuned collector circuit to the output connector. Inductors L5 thru L8 are lumped components fabricated out of 20 gauge wire turns of 0.25 inch diameters.

3.3.7 200 MHz POWER AMPLIFIER ASSEMBLY A1A9 (FIGURE 6-13)

All the components that make up the 200 MHz power amplifier circuit are mounted on a PCB, other than the feed thru capacitors and the remote POWER LEVEL CONTROL (A1R2). This PCB is enclosed in a RF shielded cover assembly. The +12 volt V_{CC} is applied via the 1000 pFd feed thru capacitor and the input and output is provided by coax connectors which are physically part of the RF cover.

The following detailed circuit analysis is supported by Figure 6-13 200 MHz Power Amplifier Schematic (C-11-09447). The input 200 MHz signal is applied to the base of transistor Q3 via the tuned input circuit consisting of L10 and C12. The resonance is tuned to 200 MHz by C12, inductor L10 consists of two turns of 20 gauge bus wire. The collector of Q3 is coupled to the base of Q2 by a series LC resonance circuit L9 and C9, capacitor C9 is adjustable and inductor L9 is constructed of two turns of 20 gauge wire. The amplifier stages formed by Q2 and Q1 are identical to Q3 other than biasing and transistor type, Q1 is a 2N6255 which can handle a higher current. The first amplifier Q3 has a fixed gain, and amplifiers Q2 and Q1 are adjustable as to gain by a remote POWER LEVEL control (A1R2) which is mounted on the auto het chassis. The POWER LEVEL control sets the output power of the 200 MHz drive to the YIG located in assembly A1A8 and is adjustable from 0.5 Watts to 1.0 Watts into the YIG's 50 ohm load. The POWER LEVEL control receives its voltage via the YIG level control transistor A1Q2 which is located on the auto het chassis near the YIG assembly and is functionally part of Power Amplifier Controller circuit located within the A1A6 plug in PCB assembly.

3.3.8 IF AMPLIFIER ASSEMBLY A1A13 (FIGURE 6-16)

The IF Amplifier Assembly is enclosed in an RF cover enclosure with the input and output connectors (J1 and J2) and the feed thru capacitors (C1 and C10) being part of the RF enclosure. All the other components are mounted on a PCB with the small chip capacitors located on the circuit (bottom)

side of the PCB.

The IF signal from the Back Diode Detector A1A15 is applied to coax connector J1 which is hard wired to the input of the 1st IF IC Amplifier (U1), a "take-off" is "T"ed and outputed via inductor L1 and fed thru capacitor C1 to the Start Detector circuit located in assembly A1A4. This signal is a dc current which is proportional to the amplitude of the applied range 3 signal and is called out in Figure 3-1 (Functional Block Diagram) as DET CURRENT.

The input IF signal is amplified by U1 and coupled via a tuned LC network (L2, L3, L4, C4, C5, C6 and C7) to the four cascaded amplifiers (U2 thru U5). A RF shield is provided between the input amplifier and the rest of the circuitry to prevent feed back which could cause the amplifier to go into oscillation. The two resistors referenced as Rx that are seriesed in the V_{CC} line are selected for value at test for maximum gain without oscillation and may range from 1 to 10 ohms in value. The output is applied via coax connector J2 to the IF shaper circuits located in PCB assembly A1A7.

3.3.9 RANGE INPUT 1 AMPLIFIER/ RANGE 2 INPUT AMPLIFIER AND DIVIDE BY 4 PRESCALER PCB ASSEMBLY A1A1 (FIGURE 6-6 SHEET 1 AND 2).

The A1A1 assembly provides the range 1 input amplifier and when the instrument is configured as a 988/989 AL model this PCB plug-in has the range 2 input amplifier and divide-by-four prescaler included. The PCB assembly plugs into the auto het mother board A1A16 which provides the interface of the operational voltages (+12V and -5.2V) and Range 1 50Ω Enable control signal. The input/output count signals are interfaced via coax connectors, the inputs are cabled from the front panel (A4) and the outputs are applied via coax cable to PCB assembly A1A2.

The RANGE 1 INPUT signal is applied to coax connector J1 and its input impedance is selected for 1 MΩ or 50Ω by the reed relay K1. When the front panel INPUT switch is placed in the RANGE 1 - 50Ω position a ground is supplied to PCB pin 10 and relay K1 will energize placing a 56Ω resistor (R1) between the input and ground. When the INPUT switch is in any other position the ground at pin 10 is removed and the reed relay (K1) will de-energize and the 56Ω shunt is removed from the 1.2 MΩ resistor (R7) effecting and 1 MΩ input impedance.

The range 1 input signal is coupled to a balanced FET amplifier (Q1 and Q2) via an input attenuator and limiter network. The signal is developed across the variable inpedance produced by the relative conduction state of the Schottky Barrier diodes CR2 and CR3. Increasing the conduction of the diodes (variable from just on to saturation) reduces the load impedance and thus increases the attenuation. Schottky Barrier diodes are used because of their fast switching time. This network performs the dual function of automatic gain control and limiting, thus preventing over driving the FET dual input amplifier.

FET transistors Q1 and Q2 are selected for gain as a matched pair and are biased to operate near their zero drift point, thus providing an essentially zero temperature coefficient and provide excellent common mode noise rejection.

Transistor Q3 a type MPS-H81 which is a Motorola® PNP silicon annular, plastic encapsulated high frequency device and is configured as a wide band amplifier, it utilizes a Schottky barrier diode (CR1) between its collector and base to increase the high frequency response of the circuit. Potentiometer (R4) is provided in Q3 emmiter circuit to adjust the gain of the range 1 preamplifier. Integrated circuit

(U1) a type MC10116 is configured as a three stage cascaded wide band amplifier limiter chain.

The range 2 preamplifier and divide by four prescaler divides the 25 - 625 MHz input signal applied to coax connector J3 by a factor of four and outputs the prescaled signal at coax connector J4 to the first DCU located on assembly A1A2. Figure 6-6 sheet 2, Range 2 Input Amplifier and Divide by 4 Prescaler Schematic (C-11-10732) is referenced to the following circuit analysis. The range 2 input circuit is comprised of a preamplifier (Q5 and Q6) which are type MMT 8015 NPN silicon RF high gain, small-signal microwave amplifiers, a divide-by-two network (Q7 thru Q25), and a divide-by-two flip-flop IC circuit (U2). The divide-by-two network comprises three differential amplifier signal steering circuits (Q7 - Q8, Q9 - Q10, and Q11 - Q12), a master flip-flop (Q17 - Q18 and Q19 - Q20), a slave flip-flop (Q13 - Q14 and Q15 - Q16), an output differential amplifier (Q23 - Q24) coupled by emitter followers (Q21 and Q22), and an output emitter follower (Q25). Figure 3-4 is a timing diagram to which the following analysis is referenced with the support of the schematic diagram Figure 6-6 sheet 2.

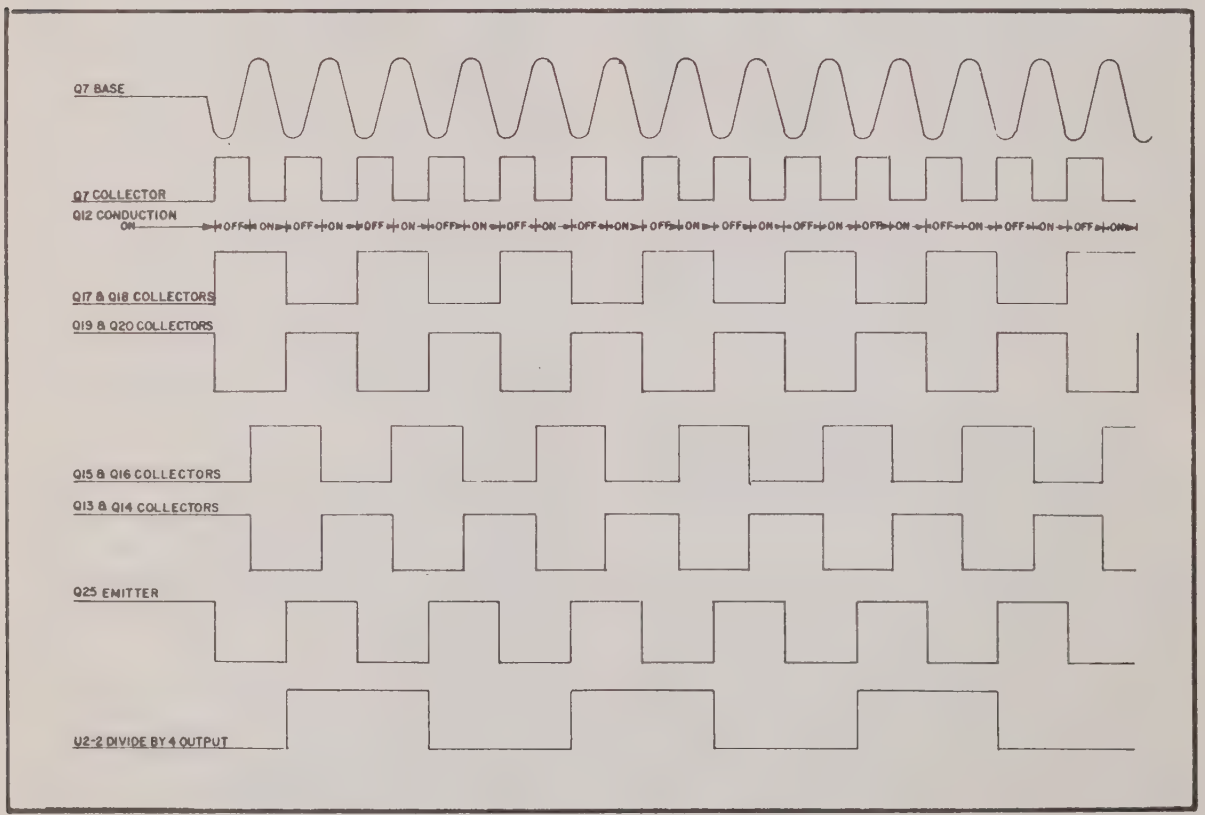


FIGURE 3-4

RANGE 2 PREAMPLIFIER AND PRESCALER TIMING DIAGRAM

Capacitor C27 couples the amplified (by cascaded Q5 and Q6) input waveform to the base of Q7, the input to the divide-by-two network. Because of the bistable nature of the divide-by-two network, any explanation of this circuit's operation must assume a static state operating condition. So, assume that prior to the application of an input waveform at the base of Q7, Q7 is on (conducting) and Q8 is off (not conduction). Then, Q10 and Q11 are off and Q9 and Q12 are on. When Q11 is off, Q17 and Q20 must be off. Likewise, when Q10 is off, Q14 and Q15 must be off. When Q12 is on, either Q18 or Q19 is on and when Q9 is on, either Q13 or Q16 is on. A this point assume, because Q12 is on, that Q18 is conducting and Q19 is not conducting (note the connection between the Q18 collector and the Q19 base). When such is the case, Q16, Q18 and Q23 have a logic high (approximately ground) on their bases (Q19 and Q20 are off) and Q13, Q19 and Q24 have a logic low (-5V nominal) on their bases (Q18 is on). Because Q9 is on, Q16 conducts (high at its base) and Q13 is off (low at its base). So, Q14 and Q17 have a logic low at their bases (Q16 is on) and Q15 and Q20 have a logic high at their bases (Q13 and Q14 are off). This completes the description of a typical divide-by-two network static state.

Upon application of an input waveform and receipt of a negative-going transition at the base of Q7, Q7 goes off and Q8 goes on which turns on Q10 and Q11 and turns off Q9 and Q12. When Q12 is off, Q18 and Q19 must be off; when Q9 is off, Q13 and Q16 must be off. When Q11 conducts, Q20 turns on (high at its base from preceding static condition) and Q17 remains off. Similarly, when Q10 turns on, Q15 conducts and Q14 remains off. At this time, the waveforms at the collectors of Q13-Q14, Q15-Q16, Q17-Q18 and Q18-Q20 are as shown in Figure 3-4 below the initial negative-going transition of the input waveform. That is, Q17 and Q18 are off; their common collector level is high. Q19 is off and Q20 is on; their common collector level is low. Q15 is on and Q16 is off; their output is low. Q13 and Q14 are off; their output is high.

Upon receipt of the first positive-going transition at the base of Q7, Q7 goes on and Q8 goes off. Therefore, Q9 and Q12 turn on while Q10 and Q11 turn off. When Q11 is off, Q17 and Q20 must be off; when Q10 is off, Q14 and Q15 must be off. When Q12 turns on, Q19 turns on (high at Q19 Q19 base from previous input waveform half cycle) and Q18 remains off (low at Q18 base from previous half cycle). Similarly, when Q9 turns on, Q13 turns on and Q16 remains off. At this time, the waveforms at the collectors of Q13-Q14, Q15-Q16, Q17-Q18 and Q19-Q20 are as shown in Figure 3-4 below the first positive-going transition of the input waveform. The process described above continues in a similar manner until receipt of the third negative-going transition at which time the cycle begins to repeat itself. Divide-by-two flip-flop U2 toggles only upon receipt of a positive-going transition at U2-Pin 7.

3.3.10 INPUT CONTROL AND 1ST DCU ASSEMBLY A1A2 (FIGURE 6-7).

The input signal gate selection logic is configured out of IC's U2, U3 and their associated components. U2 is a type MC 1663 quad 2-input "NOR" gate having internal 2 K ohm input pulldown resistors, the four gate elements have the input signals applied to one of their inputs, i.e., Range 1, Range 2, Range 3 and 1MHz Clock. The other inputs are wired to the INPUT front panel selector switch (A4S2) which applies -5.2 volts as an enable signal for the selected input or the test function (1 MHz Clock). These input selector gates are ECL logic and are pulled down to -5.2 volts at both the signal inputs and the outputs. Due to the -5.2 volts enable signal the actual logic function is negative logic "NAND" gating. The IC U3 is

a type MC 1661, ECL dual 4-input gate and element A is circuit configured as a positive logic NOR gating function which will invert any one of the selected four inputs and apply it to the 1st DCU input (U4 pin 11).

The 1st DCU is configured out of four ECL D type flip flops which is comprised of IC's U4 and U5. The 1st DCU is wired as a BCD counter by having its B and C outputs "OR"ed by U3B gate and applied to the D input of the D flip flop, and the D output (Bit "8") wired to the B flip flop input OR gate (pin 11).

IC U1 provides a TTL-to-ECL translator for the applied GATE, RESET and 1 MHz CLOCK signals. One of its four dual inputs is pulled up to +5.0 volts and its four outputs a pulled down to -5.2 volts. U1 element A provides the TTL-to-ECL logic translation for the 1 MHz CLOCK which is gated to the 1st DCU via gates U2D and U3A when the test mode is enabled. Gate U1B element provides the logic translation of the RESET signal for the resetting of the 1st DCU. Gate elements U1C and E provides the logic translation of the GATE signal, element C outputs a ECL DCU ENABLE signal and element D outputs the ECL BCD ENABLE signal to the output BCD ECL-to-TTL translator U6.

The 1-2-4-8 BCD output of the 1st DCU is applied IC U6 which is a type MC1039 ECL-to-TTL quad translator which converts the ECL (-5.2V) logic level to a TTL (+ 5.0 volts) and outputs it to the Count Chain located in assembly A2, and the D/A Converter (A1A5).

The DCU Bits "4" and "8" outputs are "OR" gated by transitors Q1 and Q2 to generate the Count Carry signal. Transistors Q3 and Q4 are configured as a ECL-to-TTL translator, the Count Carry signal is coupled to the emitter of Q3 and its collector is pulled up to +5.0V via R44, the base is returned to Vbb (pin 9 of U6). The collector of Q3 is dc coupled to the base of Q4, which is a TTL emitter follower that outputs the Count Carry signal to the Count Chain logic located on assembly A2 via the output coax connector J4.

3.3.11 SWEEP GENERATOR ASSEMBLY A1A3 (FIGURE 6-8).

The Sweep Generator receives a START signal from the Start Detector logic located within the A1A4 assembly which will initiate the generation of the sweep. A STOP signal from the Stop Detector logic located within assembly A1A7 will stop the sweep generator at a count which will effect lock on of the autohet function. The MANUAL RESET signal from the front panel push button switch (A4S4) will cause a reset to zero of the sweep counter thus allowing restart of the sweep if the START signal is present. The PRESET ENABLE signal will allow remote preset start and stop limits of the sweep's three most significant digits (MSD) by the BCD Preset Stop/Start inputs. The SWEEP OUTPUT signal in BCD format is applied to the D/A Converter (A1A5) for the generation of the YIG tuning ramp, and to the Preset "N" logic located in assembly A1A4 for the "N" number to be preset in to the count chain.

Figure 3-5 provides a functional logic diagram of the Sweep Generator and the input/output signals described in the preceding paragraph are called out as the "to" and "from" taged signals. U3A the Start/Stop Gate operates on logic high inputs thus functions as a NAND gate, when all three of its inputs are placed high (+5.0V) the output will be low (0V) generating the SWEEP GATE signal which in turn will gate on the 50 KHz Free Running M.V. and clock the Sweep Counter. When the Sweep Counter reaches a count that will effect an hetrodyning of the YIG comb line and the range 3 input signal, the STOP signal will go low and in turn place the Start/Stop gate (U3A) output high and gate off the

50 kHz MV thus stopping the Sweep Counter. At the same time the STOP signal is inverted by U1E to a high and applied to the Control "NOR" gate (U3B) thus outputting a CONTROL ENABLE signal which will allow the STOP/START logic to drop the START ENABLE signal which will in turn lock out the Start/Stop gate (U3A) to insure that "auto het lock on" is maintained. It should be noted that the START signal that is inverted by U1F to a START signal is a complement of the STOP signal both logically and in level and will effect the Control gate (U3A) in the same way as the STOP signal.

When a manual reset is initiated by the front panel RESET push button switch (A4S4), the MANUAL RESET signal is placed low (0V) and the Sweep Stop/Start, Reset logic will drop the START ENABLE signal for a period of 5 μs and generate the RESET signal which is applied to the Sweep Counter to reset the counter to all zero's. After the 5 μs delay period the Sweep Generator will restart its count if the START signal is high.

When the PRESET ENABLE signal is placed high, the preset logic will drop the START ENABLE signal and generate the PRESET signal which will allow the PRESET START INPUTS (BCD) to preset the Sweep Counter's three MSD in accordance with its BCD format. The Sweep Preset BCD inputs are wired from the rear panel's SWEEP PRESET Connector (A5J3) to IC socket (J1) on the Sweep Generator's PCB (A1A3). Five μ seconds after counter preset the START ENABLE signal will go high and allow the Sweep Counter to count up from its preset number.

A PRESET STOP signal is generated when the SWEEP OUTPUT (BCD) signal compares with the SWEEP PRESET STOP INPUT (BCD) signal. This PRESET STOP signal is developed by the Preset Stop Comparator

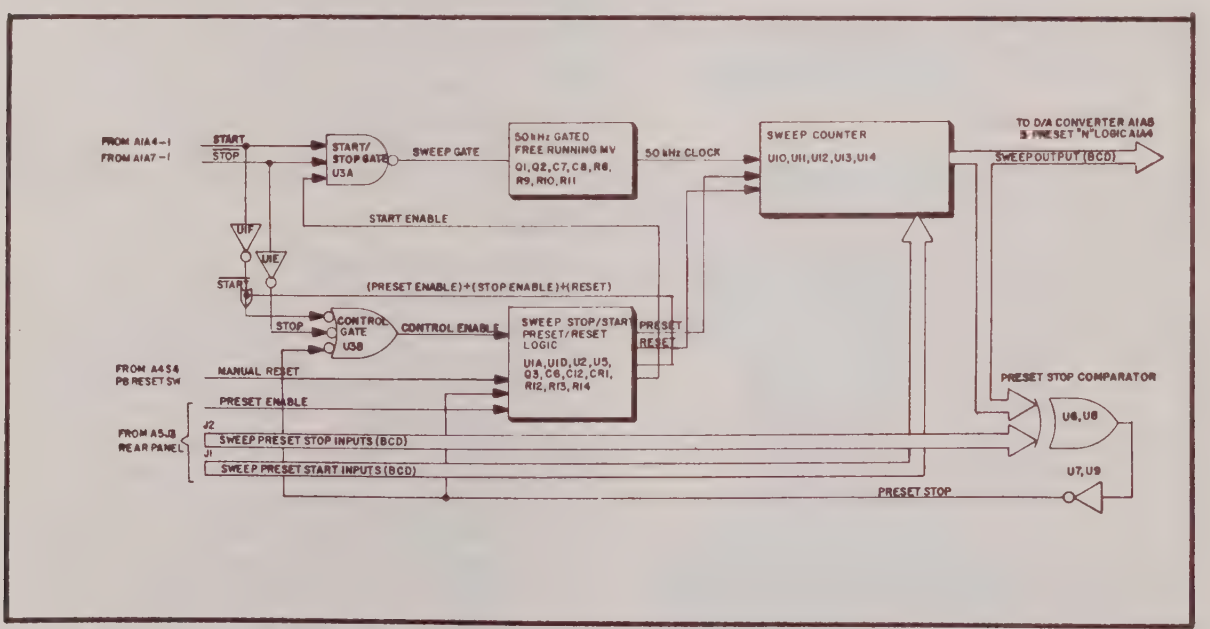


FIGURE 3-5

SWEEP GENERATOR FUNCTIONAL LOGIC DIAGRAM

logic (U6 thru U9), which is configured out of nine two-input exclusive-OR-gates and nine inverters. The PRESET STOP INPUTS (BCD) signal is a logic low (0V) and the SWEEP OUTPUT (BCD) signal is outputed as a high (+5.0 V), thus when they are complementary the nine exclusive OR gates performs the logic operation of $Y = A \oplus B$ ($Y = \overline{A}B + A\overline{B}$) and are combined (OR'ed) at the common inverters output tie point generating the PRESET STOP signal. The $\overline{\text{PRESET STOP}}$ signal is gated with the PRESET ENABLE signal which in turn will drop the START ENABLE signal, reset and preset the Sweep Counter, and after a 5 μ second period return the START ENABLE signal high allowing the counter to count up from its preset number if the START signal is high.

3.3.12 START DETECTOR AND PRESET "N" LOGIC ASSEMBLY A1A4 (FIGURE 6-9)

The A1A4 assembly contains circuitry for two unrelated logic functions, the Start Detector circuit and the Preset "N" Generator logic.

The Start Detector circuit generates a START signal which will initiate the YIG tuning sweep on the presence of a range 3 input, and supplies meter drive to the RANGE 3 INPUT LEVEL meter (A4M1). DETECTOR CURRENT (DIODE CURRENT called out in figure 6-9) from the IF Amplifier's A1A13 "take off" circuit flows through the front panel RANGE 3 LEVEL meter (A4M1) via transistor Q1 and IC operational amplifier U12. The variable resistor (R5) METER ADJ control provides for the calibration of the meter's deflection and is normally set to provide half scale deflection of the meter with a 200 mV 3 GHz test signal applied to the range 3 input connector. The output of IC amplifier U12 is also applied to the non-inverting input of operational amplifier U11 which provides the Start Detector function. When the RANGE 3 ENABLE signal (called out as BAND 3 ENABLE on figure 6-9) is placed low (0V) by the front panel INPUT switch (A4S2) a Start Detector Enable is generated by transistor Q2 and applied to pin 9 of U11, which effectively removes the offset and enables the operational amplifier. The inverted input of the amplifier (U11 pin 2) is connected to a voltage divider network that is adjustable by the START LEVEL control (R10) and is normally set to provide a START signal output at U11 pin 6 when the input RANGE 3 signal applied to the front panel connector (A4J3) is greater than 100 mV (-3 dBm). The START signal is outputed via A1A4 PCB pin 1 to the Stop Detector circuit (A1A7) and the Sweep Generator (A1A3).

The Preset "N" logic generates a serial 500 kHz gated clock which its number of clock pulses equals the preset "N" number. This preset "N" count is applied to the Count Chain (A2 assembly) to preset the counter to the "N" number when auto het lock on is achieved. Figure 3-6 Preset "N" Functional Logic Diagram and the A1A4 assembly Schematic Diagram. Figure 6-9 supports the following analysis of the preset "N" number generation and logic functions.

A 1 MHz CLOCK signal is applied to the first flip flop input of DCU U4 at pin 14, the divide-by-two output A which is a 500 kHz clock (U4 pin 12) is then applied to one of the three inputs of the Preset "N" Count Gate (U1A pin 13). When the auto het converter is "locked-on" the $\overline{\text{STOP}}$ signal will be present as a low and is inverted to a high (+5 volts nominal) by inverter U5B and applied to U1A pin 1. At this mode state the preset "N" counter is reset to zero and a high is present on pin 2 of U1A. The Preset "N" Count gate (U1A) when thus enabled outputs a 500 kHz clock which is inverted by U1C and applied to the Preset "N" Counter (U2 pin 14, and the Exclusive-OR-gate (U8C pin 13). The exclusive-OR-gate (U8C) allows

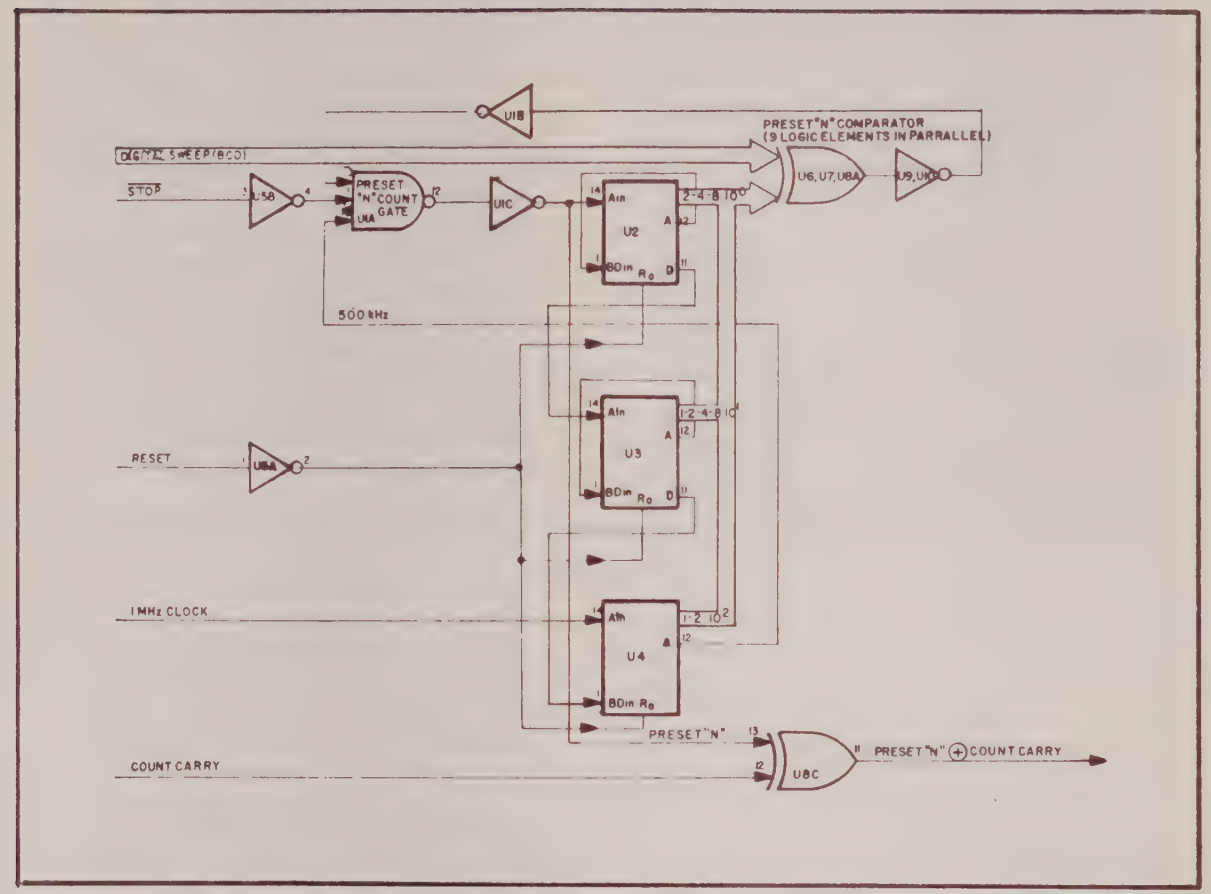


FIGURE 3-6

PRESET "N" FUNCTIONAL LOGIC DIAGRAM

the 500 kHz Preset "N" to be gated out to the Count Chain (A2). The Preset "N" BCD Counter is configured by IC type SN 7490 DCU'S U2, U3, and the B-C-D flip flops stages of U4 (the A flip flop of U4 is used for the ÷ 2 500 kHz generation function described previously). The Preset "N" BCD Counter when clocked by the 500 kHz signal will count up and output is running count via nine lines to the Preset "N" Comparator circuit in the following format.

Bit "2" 10^0_0	U2 pin 9
Bit "4" 10^0_0	U2 pin 8
Bit "8" 10^0	U2 pin 11
Bit "1" 10^0_1	U3 pin 12
Bit "2" 10^1_1	U3 pin 9
Bit "4" 10^1_1	U3 pin 8
Bit "8" 10^1_2	U3 pin 11
Bit "1" 10^2	U4 pin 9
Bit "2" 10^2	U4 pin 8

The Preset "N" Comparator is configured from nine 2-input exclusive-OR-gate elements feeding nine inverter elements that are "OR"ed at a common tie point. (refer to figure 6-9 for the actual schematical configuration of the circuit). Functionally the comparator is a nine element complementary exclusive OR gate outputting a high (5 volts nominal) at the common

inverter "OR"ed tie point when the Preset "N" BCD Counter's output equals the Digital Sweep BCD complementary count. The comparator output is inverted to a low by inverter 1UB that gates off the 500 kHz clock when the Preset "N" count equals the DIGITAL SWEEP count.

In summation the Preset "N" generator is basically a nine-line BCD-to-serial converter outputting a train of 500 kHz pulses which total count equals the BCD Sweep "N" number, this serial output clocks the Count Chain to preset the "N" number in the three MSD of the counter. Exclusive OR gate U8C provides the function COUNT CARRY⊕PRESET "N" to the Count Chain's three MSD.

3.3.13 D/A CONVERTER ASSEMBLY A1A5 (FIGURE 6-10)

The purpose of the Digital-to-Analog (D/A) Converter is to provide a analog YIG tuning ramp to the YIG Driver/ Controller (A1A6) which when converted to a current drive will magnetically tune the YIG to the proper harmonic and thus provide the auto het lock on and derive the "N" preset number. Figure 3-7 the A/D Converter Functional Block Diagram and Figure 6-10 A/D Converter Assembly (A1A5) Schematic Diagram support the following detailed description.

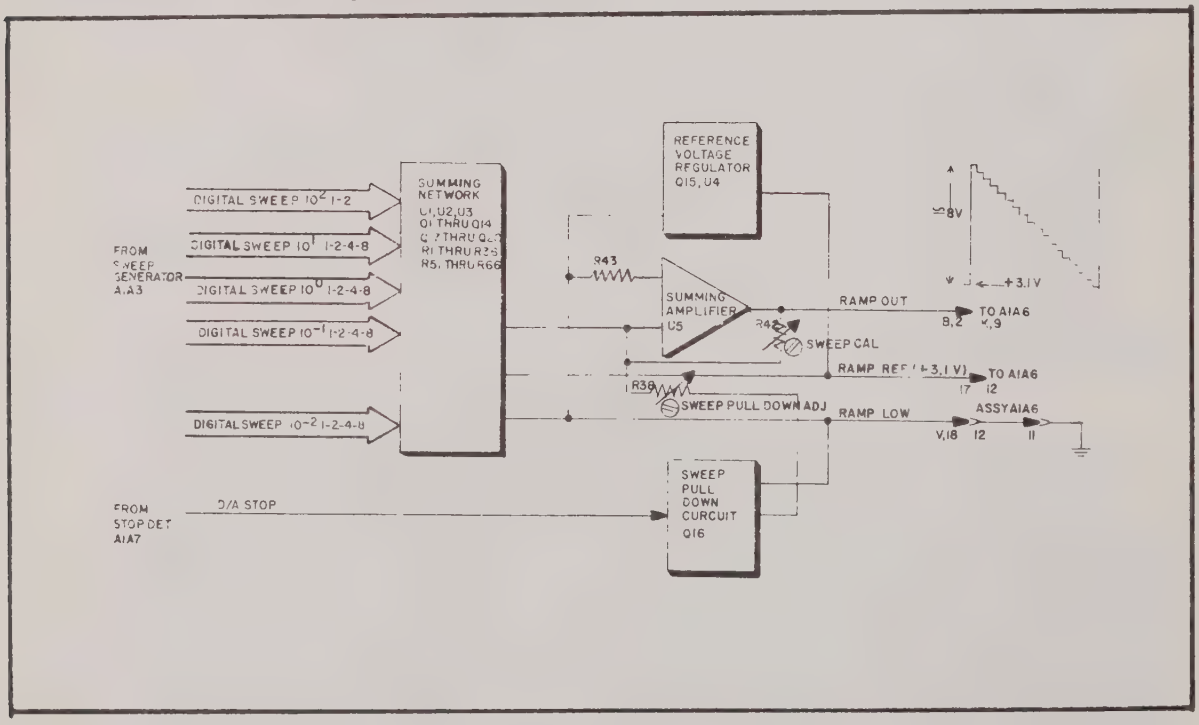


FIGURE 3-7

A/D CONVERTER FUNCTIONAL BLOCK DIAGRAM

The D/A Converter receives BCD weighted digital inputs from the Sweep Generator Assembly (A1A3) via eighteen lines which are inverted by three hex inverters IC's (U1, U2, and U3) and applied to the 18 step summing network. This summing network is a resistive ladder which adds its effective resistive elements in parallel when a high is placed on the associated control transistor base. The summing network is configured by control transistors Q1 thru Q14 and Q17 thru Q20 and the associated resistors, R1 thru R36 and R51 thru R66 (refer to schematic figure 6-10). The summing resistors are of high tolerance (± 0.02% and ± 1%) and have a low temperature coefficient (± 10 PPM/°C and ± 50 PPM/°C). One side of the network is referenced to + 3.1 volts (nominal) at the common collector tie point by the reference voltage regulator. The other side of the network is applied to the inverting input of the summing amplifier (U5 pin 2) the non-inverted input (U5 pin 3) is reference to RAMP LOW via R43 a 4.99 KΩ 1% resistor. The RAMP LOW line in turn is reference to ground (0 volts) via assembly A1A6 to a ground point located near the YIG on the auto het chassis, electrically its the ground side of A1R1 the 4Ω 25 Watt YIG tuning coil return resistor.

The gain of the summing amplifier is adjustable by the SWEEP CAL adjustment poteniometer (R45) which is adjusted to provide a output ramp that will tune the YIG to its upper limit when all 18 digital input bits are high. This control is set to provide a 13.4 GHz frequency limit for the Model 988 or 18 GHZ for the Model 989. When auto het lock-on is achieved a D/A STOP signal generated by the Stop Detector Logic (part of A1A7) and applied to A1A5 PCB pin 19 will initiate the sweep pull down circuit (Q16), the circuit decreases the YIG tuning ramps amplitude by a small amount which is adjustable by poteniometer R38. Its function is to compensate for the YIG hystersis caused by the remnant magnetic flux which produces a small overshoot of the YIG tuning. The D/A Converter output consists of three lines, RAMP, REFERENCE and LOW. The RAMP is the cursive step signal which will tune the YIG as referenced to the + 3.1 volt REFERENCE level, and the LOW is the ground line which is referenced to a single-point ground located at the YIG tuning current chassis return ground point.

3.3.14 YIG DRIVER AND POWER AMPLIFIER CONTROLLER ASSEMBLY A1A6 (FIGURE 6-11)

The YIG Driver and Controller provides two operational functions. One being the improvement of the YIG ramp, drive linearity and the control of the low end start set point. The other function is the development of a control signal which will vary the output drive of the 200 MHz Power Amplifier (A1A11) in direct relationship to the YIG ramp drive.

The YIG ramp from the D/A Converter Assembly (A1A5) consisting of three lines; RAMP HIGH, RAMP LOW, and RAMP REF is applied to the YIG driver circuits consisting of operational IC amplifiers U1, U2 and emitter follower Q1 and their associated components. Control R13 called out as LOW FREQ (TUNING) adjusts the amplitude of the RAMP REF signal applied to the inverting (-) input of operational amplifier U1 and will effect the starting offset of the YIG drive thus determining the frequency of the low comb line of the YIG (this control is normally set to provide a 0.4 GHz low comb line). The BREAK control (R2) adjusts the voltage level applied to the noninverting (+) input of operational amplifier U2 and sets the "break point" of the linearizer circuit. As the ramp level increases in relationship to its corresponding frequency, the linearity of its slope is degraded by rolloff above 12 GHz tuning point. Figure 3-8 depicts the YIG drive signal to the YIG Tuned Multiplier showing the effect of the linearizer circuit. The linearizer

output from Q1 compensates for the roll-off at the > 12 GHz point. The two nonlinear signals will tend to cancel and produce the resultant linearized output to the YIG Driver transistor (A1Q1) located on the auto het chassis.

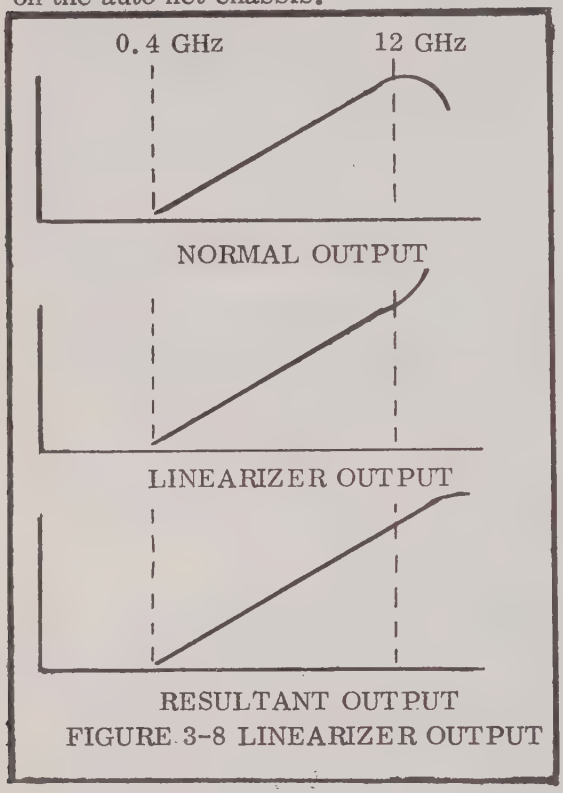


FIGURE 3-8 LINEARIZER OUTPUT

The power amplifier controller circuit is comprised of operational amplifier U3 and emitter follower Q2 and associated circuit components. The RAMP HIGH signal from the D/A Converter (A1A5) is applied to the inverting input (-) of U3, and the noninverting input (+) is set to a level of ≃ -3 volts by the voltage divider network (R18 and R19). The gain of the operational amplifier U3 is set by the 18 KΩ resistor or the LEVEL control 30K potentiometer (R17) and determines the amplitude of the ramp signal that is outputted to the Power Level Control Transistor A1Q2 via the emitter follower Q2 and zener diode VR1. The chassis mounted Power Level Control A1R2 and the Power Level Control Transistor A1Q2 determines the V_{CC} voltage applied to the second and third amplifier stages of the 200 MHz Power Amplifier (A1A9), (refer to the figure 3-1 and 6-16 for the interconnect relationship of the 200 MHz Power Amplifier level control function).

On the Model 988/989 A (L) serial number # 746 and above series, the linearizer circuit has been deleted and the following components have been removed from the A1A6 assembly; U2, Q1, CR2, R1, 2, 5, 6, 8, 9 and 10. Also effected by this series change is the LEVEL control R17, that has been replaced by a fixed 18K Ω resistor.

3.3.15 STOP DETECTOR AND IF SHAPER ASSEMBLY A1A7 (FIGURE 6-12)

The Stop Detector Circuits provides for the generation of the STOP, D/A STOP and LOCK command signals. The shaping of the IF signal for presentation to the 1st DCU located in assembly A1A2 as an ECL Compatible count, is the function of the IF Shaper circuit.

The Stop Dectector acquisition circuits are comprised of three threshold detector-comparators followed by gating logic for the generation of the command signals. Figure 3-9 provides a functional logic diagram of the Stop Detector and IF Shaper circuits, and the following detailed cirucit analysis relates to this figure and Figure 6-12, the schematic diagram located in Section 6 of this manual.

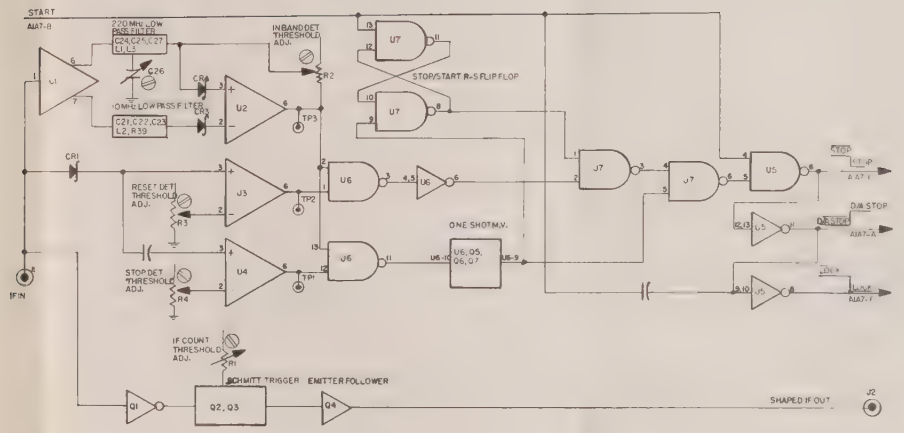


FIGURE 3-9A
STOP DETECTOR AND IF SHAPER FUNCTIONAL LOGIC DIAGRAM

The In Band Detector circuit will generate a logic high at test point TP3 when a hetrodyne IF related signal between 10 MHz and 220 MHz is present at the IF IN connector (J1). The IF signal is applied to U7 which is a IC type CA3049 dual independent differential amplifier (see Type CA3049 IC data sheet in section 6 for its detailed configuration). The IF input is applied to input pin 1 of the first stage, and its other input (pin 10) is set at a offset by divider network R2, R5 and R11 which sets the fixed threshold of the first stage. The first stage outputs (pins 12 and 11) are connected to the second stage inputs (pins 7 and 4) which are clamped by zener diode CR3 at +8.2 volts, which will limit the amplifiers gain. Second stage outputs (pins 5 and 6) parallelly feed the lowpass filters. The 220 MHz lowpass filter is adjustable as to its upper end cutoff frequency by C25. The 10 MHz lowpass filter is fixed as to its cutoff frequency. The 220 MHz and 10 MHz lowpass filter outputs are detected by two type HP2800 Schottky-barrier diodes (CR7 and CR6 respectively) and applied to the inputs of differential amplifier IC U5 (pins 3 and 2). When the difference in the detected levels exceeds the offset set by the IN BAND DET THRESHOLD ADJ control (R50), which is normally set to place U5 pin 3, 30 mV more negative than U5 pin 2, the output (pin 6) will go to a logic high. This high at the output of the detector indicates that the IF signal is between 10 MHz and 220 MHz in frequency.

The Reset Detector circuit will generate a logic low at test point TP2 when the IF signal detected by CR5 drops to a level that is less than the offset set at U6 pin 2 by the RESET DET THRESHOLD ADJ control (R35). This offset is normally set to provide reset detection when the IF signal level at J1 is less than -70 dBm.

The Stop Detector circuit will generate a logic high at test point TP1 when the IF signal detected by diode CR5 and ac coupled to pin 3 of U4 exceeds the offset set by the STOP DET THRESHOLD ADJ control (R40) on pin 2 of U4. Normally R40 is adjusted to provide detection when the IF signal is greater than -60 dBm in level.

When a logic high is present at test point TP3 indicating that the IF signal is within the band (between 10 MHz and 220 MHz), and a high is present at test point TP1 indicating that the signal is greater than the threshold level (> -60 dBm), pins 13 and 12 of U1 NAND gate will be at a logic high. The NAND gate output (U1 Pin 11) will go low and trigger the one shot M.V., which in turn outputs a negative 10 ms pulse. The 10 ms logic low pulse is applied to the STOP/START flip flop at U2 pin 9 and NAND gate input U2 pin 5. If the START signal is high at U2 pin 13 the 10 ms logic low gate from the one shot M.V. will set the STOP/START flip flop and its output (U2 pin 8) will go high. When the START/STOP flip flop is set, pin 1 of NAND gate U2 is placed at a logic high and if the reset threshold has not dropped (low at TP2), U2 pin 2 will also be at a logic high, and a low will be present at U2 pin 4. When the 10 ms logic low from the one shot M.V. is present at U2 pin 5 the gate is disabled with a logic high output at U2 pin 6 and U3 pin 5. U3 pin 4 is set at a logic high by the START signal thus the gate will be enabled and generate the $\overline{\text{STOP}}$ command (logic low) at U3 pin 6. The $\overline{\text{STOP}}$ signal is inverted and outputted at U3 pin 11 as the D/A STOP command. The D/A STOP signal is also applied to pins 9 and 10 of U3 and inverted generating the $\overline{\text{LOCK}}$ command signal at pin 8 of U3.

Both the $\overline{\text{STOP}}$ and $\overline{\text{LOCK}}$ signals will remain at a logic low as long as the detected IF input signal remains with in band and is above the reset level (-70 dbm) and the START signal is high. If the start signal is dropped (to a logic low), the in band detector indicates a out of band condition (logic low at TP3), or the IF

Page 3-26 para. 3.3.15 Stop Detector and IF Shaper Circuits. Two versions of this circuit are in production Functional they are the same and in most cases the PCB's are inter-changable. The Functional Block Diagram Figure 3-9 and the Schematic Figure 6-12 are described in para. 3.3.15. The following describes Functional Block Figure 3-9A and Schematic Figure 6-12A.

3.3.15A STOP DETECTOR AND IF SHAPER ASSEMBLY A1A7 (FIGURE 6-12A)

The Stop Detector and IF Shaper Circuits provide for the generation of the STOP, LOCK, and D/A stop (if appropriate) command signals and shaping of the IF signal, for presentation to the 1st DCU, as digital count.

The Stop Detector acquisition circuits are comprised of three threshold dectector-comparators followed by gating logic for the generation of the command signals. Figure 3-9A provides a functional logic diagram and Figure 6-12A the schematic description.

The IN Band Detector circuit will generate a logic high at TP3 when a heterodyne IF related signal between 10 MHz and 220 MHz is present at J1 the IF input connector. The IF signal is applied to U1 an integrated circuit type CA3102E Dual Differential Amplifier. The IF input is ac coupled via C13 to the first stage of U1 at pin 1. The opposite input to the differential, pin 4, is set at a fixed level by voltage divider R19 and R25. The first stage threshold at pin 2 is fixed by voltage divider R23 and R31. The first stage outputs, pins 14 and 13, are connected to the second stage inputs pins 8 and 11 respectively. The second stage inputs are clamped by zener diode CR2 at + 8.2 volts to limit the amplifiers gain. The parallel outputs from the second stage, pins 6 and 7, feed the lowpass filters. The 220 MHz lowpass filter is adjustable as to its upper end cutoff frequency by C26. The 10 MHz lowpass filter is fixed as to its cutoff frequency. The two lowpass filter outputs are detected by two type HPA2800 Schottky-barriar diodes (CR3 and 4) and applied to Op Amp U2 pins 3 and 2 respectively. When the difference in the detected levels exceeds the offset set by R2, the IN BAND DETECTOR THRESHOLD ADJ, the output pin 6 goes to a logic high. The IN Band Detector Threshold is normally set to place U2 pin 3, 30 mV more negative than U2 pin 2. This high at the output of the detector indicates that the IF signal is between 10 MHz and 220 MHz in frequency.

The Reset Detector circuit will generate a logic low at TP2 when the IF input signal detected by CR1 drops to a level that is less than the offset set at U3 pin 2 by the RESET DETECTOR THRESHOLD ADJ R3. This offset is normally set to provide reset detection when the IF input signal level at J1 is less than -70 dBm.

The Stop Detector circuit will generate a logic high at TP1 when the IF signal detected by CR1, and ac coupled (C35) to U4 pin 3, exceeds the offset, set by the STOP DETECTOR THRESHOLD ADJ R4, on U4 pin 2. Normally this offset is set to provide detection when the IF signal at J1 is greater than -60 dBm.

When a logic high is present at TP3, indicating that the IF input signal is within the high low band (between 10 MHz and 220 MHz), and a high is present at TP1 indicating that the signal level is greater than the threshold level (> -60 dBm), both inputs (pins 12 and 13) to NAND gate U6D are true and the gate turns on. The NAND gate output pin 11 goes low to initiate a trigger to the One-shot multivibrator. U6C, Q5, 6 and 7 and associated circuitry comprise a 10 ms One-shot M.V. which when triggered puts out a 10 ms logic low to U2 the Start-Stop flip-flop. U7C and D (a type 7400 integrated circuit) is wired in an RS Flip-flop configuration. The 10 ms low output from the One-shot is applied to U7 pin 9 and to NAND gate U7B pin 5. If the START signal at U7D pin 13 is high the One-shot 10 ms low will trigger the Start-

Stop flip-flop to the set state and its output at U7C pin 8 will go high. Setting the Start-Stop flip-flop applies an enable level to pin 1 of NAND gate U7A. If the reset threshold, level at TP2, has not dropped U7 pin 2 will also be enabled and the set output signal from the Start-Stop flip-flop will appear as an enable low input to U7B pin 4. With the 10 ms low output from the One-shot M.V. at U7B pin 5 and a low at U7B pin 4 an enabling high is present at U7's output pin 6 to the Start/Stop gate U5B pin 5. U5B pin 4 is also at a logic high by the START signal thus the gate will generate the STOP command signal, logic low at U5 pin 6. The STOP signal is inverted and outputted at U5 pin 11 as the D/A STOP. The D/A STOP signal is applied to U5B (pins 9 and 10) and is inverted to become the LOCK command signal at pin 8.

Both the STOP and LOCK signals will remain at a logic low as long as the detected IF input signal, remains in band, (between 10 MHz and 220 MHz), is above the reset level (-70 dBm) and the START signal is high. If the START signal goes low, or the IN band detector indicates an out of band condition (low at TP3), or the IF signal level drops below -70 dBm the output at U5 pin 6 will go high and effect the command output signals. This condition will allow the instrument to drop its lock and re-instate YIG scan when the START signal goes high.

The IF Shaper circuit consists of a wide band input amplifier (Q1), a schmitt trigger (Q2/Q3) and an emitter follower (Q4). The IF input (IF IN) applied to J1 is amplified by the single stage wide band amplifier and coupled to a common emitter schmitt trigger. The IF COUNT THRESHOLD ADJ (R1) sets the trigger level and the digital output (SHAPED IF OUT) is applied via the emitter follower (Q4) and output coax connector (J2) to the 1st DCU (A1A2 assembly) as an ECL compatible digital count.

. . . . . .

APPLICABLE CHANGES TO SECTION 4 RELATIVE TO THIS ADDENDUM

To apply alignment procedure as outlined in Table 4-5 make the appropriate changes to the component callouts as noted below. Figure 4-3 can be referenced for both PCB's if the TP locations are noted and the callout changes applied.

Page 4-9 Step 5 line 2 change to read "output level. Adjust the IF COUNT THRESHOLD control (A1A7R1)"

Page 4-9 Step 6 line 2 change to read "voltage at A1A7U2 pin 2"

Page 4-9 Step 6 line 3 change to read "reading. Place the Digital Voltmeter's Test probe on A1A7U2"

Page 4-9 Step 6 line 5 change to read "(A1A7R2) for"

Page 4-9 Step 6 line 6 change to read "the level measured at A1A7U2 pin 2"

Page 4-10 Step 8 line 2 change to read "(A1A7C26) for an oscilloscope"

Page 4-10 Step 9 line 8 change to read "value of A1A7R42"

Page 4-10 Step 11 line 4 change to read "RESET DETECTOR THRESHOLD control A1A7R3 in"

Page 4-11 Step 12 line 4 change to read "Rotate the STOP DETECTOR THRESHOLD ADJ control A1A7R4"

Page 4-11 Step 14 line 7 change to read "control (A1A7R4) one"

signal drops below -70 dBm (reset condition, logic high at TP2), U2 pin 3 will go low and effect the dropping of the command output signals. This condition will allow the instrument to drop its lock on and reinstate YIG scan when the START signal is high.

The IF Shaper circuit consists of a wide band input amplifier (Q1), a Schmitt trigger Q2 and Q3 and a emitter follower (Q4). The input IF signal (IF IN) applied at J1 connector is amplified by a single stage wide band amplifier and coupled to a common emitter Schmitt trigger. The IF COUNT THRESHOLD ADJ (R20) sets the triggering level and the digital output (SHAPED IF OUT) is applied via the emitter follower (Q4) and output coax connector (J2) to the 1st DCU (located in assembly A1A2) as a ECL compatible digital count.

3.3.16 1 MHz REFERENCE OSCILLATOR ASSEMBLY A7.

The standard 1 MHz Reference Oscillator assembly is a temperature controlled crystal oscillator in a self contained (black box) assembly that provides 1 MHz reference output to the Clock Control Logic assembly (A6) with a stability of:

Short Term: 7×10^{-9}/day (after 30 days aging)
Long Term: 3×10^{-8}/week (after 30 days aging)
Temperature: 5×10^{-9}/°C (from 0 to 50° C)

This assembly is a sealed unit, EE part number 5895-003291 and manufacturer's part number Ovenaire® 22-16B and for purposes of maintenance is treated as a black box.

The internal heater element is supplied 115 vac directly from the load side of the instruments line fuse (A5F1) thus allowing the Reference Oscillator internal oven to remain operational when the instrument is plugged into the line source regardless of the setting of the front panel POWER OFF/ON switch. The V_{ee} -12 vdc is supplied to the oscillator from the Power Supply Assembly (A3), and the 1 MHz output is applied via coax cabled to the Clock Control assembly (A6) located near the rear panel. When option E is configured into the instrument the standard oscillator assembly is replaced by a 10 MHz Austron ®1100-2 assembly (EE part number 5895-003119) which provides a greater stability which is specified as follows:

Short Term: 5×10^{-10} peak to peak for 7 minutes
Long Term: 1×10^{-9}/day (after 48 hours aging)
Temperature: 2×10^{-10}/°C (from 0° - 50°C)

This optional reference oscillator requires +28 volts for the internal oven and when optioned a +28 volt regulated power supply is added to the Power Supply assembly A3 (see figure 6-19 Power Supply Assembly Schematic Diagram).

Both the standard 1 MHz and optional 10 MHz Reference Oscillators are provided with a FREQUENCY ADJ controls to allow calibration of the oscillator with a 1 MHz frequency standard (refer to Section 4 calibration procedures for reference oscillator test and calibration).

3.3.17 CLOCK CONTROL ASSEMBLY A6 (FIGURE 6-2)

The Clock Control assembly is a printed circuit board (P, C, B,) mounted near the instruments rear panel assembly (A5). It receives a 1 MHz Reference Clock (10 MHz when E or D option is installed) and fans out three 1 MHz clock signals to the instruments major functional circuits, and provides an external clock to the rear panel 1 MHz connector when the INT/EXT switch is placed in the INTernal position.

Unregulated +5 vdc (RAW +5) is supplied from the Power Supply assembly (A3) via a twisted pair to IC U1 a type MC309H voltage regulator. The regulated +5 volt V_{cc} is outputed at U1 pin 2 and applied to the IC DIP's of the Clock Control assembly.

The input 1 MHz (or 10 MHz) reference signal (OSC INPUT) from assembly A7 is applied to coax connector J4 and is buffered and inverted by IC U3 element F then applied to pin 1 of IC U2. Integrated circuit U2 a type SN 7490 decade counter will divide the 10 MHz reference clock by a factor of 10 when option D or E is installed in the instrument, outputting a 1 MHz clock at pin 11. When the standard Reference Oscillator is used a jumper is wired between pins 1 and 11 of U2 thus bypassing the ÷ 10 counter function. U2 pin is connected to two inverters in parallel configuration (elements D and E of U3) which provides the drive to the base of transistor Q1 when the INT/EXT switch is placed in the INTernal position. When the INT/EXT switch is placed in the EXTernal position the OSC INPUT signal from the reference oscillator A7 is grounded thru 47 ohm (R4) and the source for transistor Q1 base is the rear panel 1 MHz coax connector, thus allowing a remote 1 MHz frequency reference to be used. Transistor Q1 collector outputs to three inverters (U3 elements A, B and C) which provides the reference clock fan out. Listed below is the 1 MHz clock distribution and its interfaces.

Connector	Signal	Destination
A6A1J1	1 MHz TIME BASE CLOCK	A2 pad 8
A6A1J2	1 MHz AUTO HET CLOCK	A1A16 pad
A6A1J3	1 MHz PHASE LOCK CLOCK	A1A12 input Connector
A5J5	1 MHz Monitor/1 MHz Ext	External

3.3.18 MAIN COUNTER AND DISPLAY ASSEMBLY A2

The Main Counter and Display group is a assembly comprised of a 4.25" x 5.50" printed circuit board mounting 77 IC dual-in-line packages (DIP's), the 11 display tubes and a number of discrete components. The A2 assembly circuitry is divided into four functional sub-groups (see figure 3-1 Model 988/989 Functional Block Diagram, for the functional sub-grouping and their interface). For the purpose of circuit analysis each sub-group is discussed separately and is supported by its own specific schematic diagram. Listed below are the functional sub-groups, their schematic drawing number, and figure number.

Functional Name	Schematic Dwg. No.	Figure No.
TIME BASE LOGIC	D-11-09585	6-1
CONTROL LOGIC	D-11-09582	6-3
COUNT CHAIN	D-11-09587 (Sheet 1 and 2)	6-4
STROBE DISPLAY LOGIC	D-11-10123	6-5

TIME BASE LOGIC (FIGURE 6-1) The Time Base logic counts down the 1 MHz TIME BASE CLOCK signal to generate two outputs, a 10 kHz clock (for the clocking of the strobed display logic), and a count gate ($\overline{\text{CLOCK}}$) which will gate on the main counter for the required period. The $\overline{\text{CLOCK}}$ period is determined by the input $\overline{\text{PRESCALE}}$ and 10 $\overline{\text{kHz}}$ control signals. Figure 3-10 provides a functional logic diagram of the time base functions and the following detailed analysis is related to this figure.

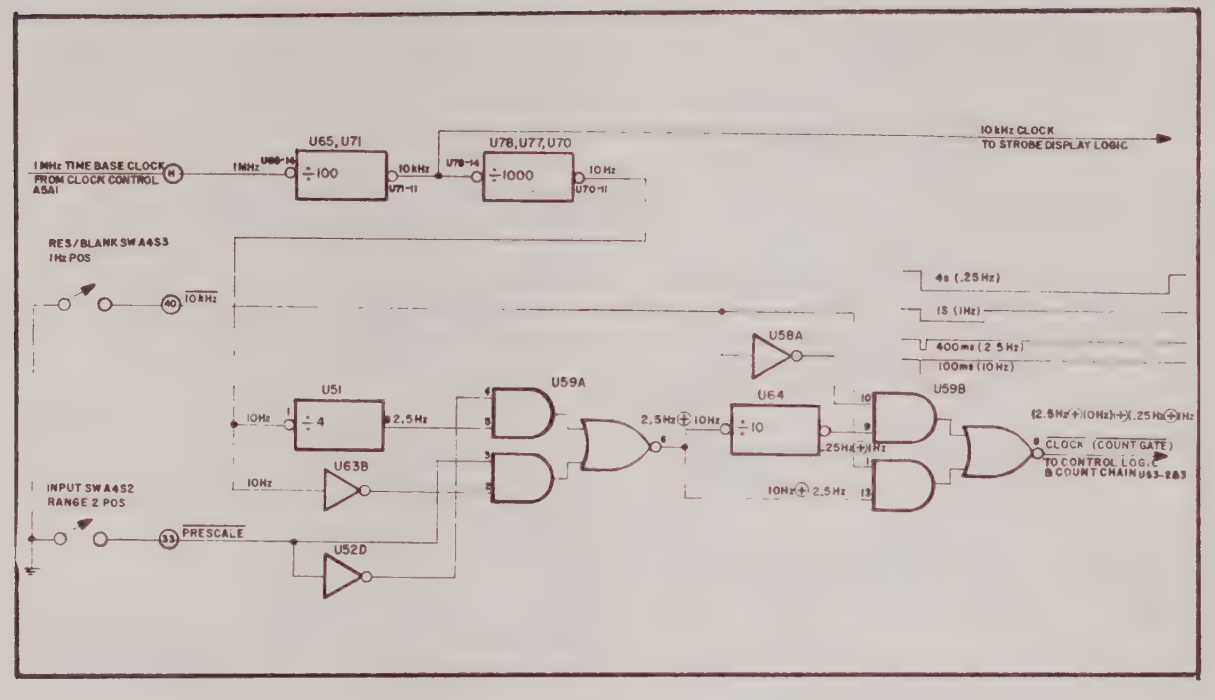


FIGURE 3-10

TIME BASE FUNCTIONAL LOGIC DIAGRAM

The divide by ten (÷ 10) counters U65, U71, U78, U77, U70 and U64 are IC types SN7490 and are configured as ÷ 10 counters by externally connecting D output (pin 11) to the A input (pin 12) of each IC. The divide by four counter U51 is a IC type SN 7473 dual J-K flip flop and is configured as a ÷ 4 counter by connecting the first flip flop's $\overline{Q}$ output (pin 13) to the second flip flop's clock input (pin 5) and taking the ÷ 4 output at the second flip-flop Q output (pin 8).

The 1 MHz TIME BASE CLOCK which is referenced to the Reference Oscillator assembly A7 signal is applied to the clock input pin 14 of U65 and counted down to 10 kHz by the ÷ 100 counter (U65 and U71 in cascade), and outputted to the Strobe Display Logic. This 10 kHz clock is also applied to three ÷ 10 decade counters in cascade (÷ 1000 chain comprised of U78, U77 and U70) which outputs a 10 Hz clock to U51 pin 1 the ÷ 4 counter, and inverter U63B. When the front panel INPUT switch (A4S2) is placed in the RANGE 2 position, a logic high is set at pin 4 of gate U59A (inverted from a low by U52D) and a logic low is set on pin 3 of U59A, thus enabling the 2.5 Hz clock output at pin 6 of gate U59A. When the INPUT switch is placed in any position other than RANGE 2 the PRESCALE control signal will be disabled (set at a logic high) and U59 pin 4 will go low and pin 3 will be set to a logic high, enabling the 10kHz clock at U59 pin 6. The switch selected 2.5 Hz ⊕ 10 Hz clock is applied to pin 14 of U64 ÷ 10 Counter and to pin 13 of gate U59B. The ÷ 10 counter U64 counts down the 2.5 Hz ⊕ 10 Hz clock to a .25 Hz ⊕ 1 Hz clock and applies it to pin 9 of gate U59B. When the front panel RESOLUTION/BLANKING switch (A4S3) is placed in the 1 Hz position a logic low $\overline{10\ kHz}$ control signal is applied to pin 1 of gate U59B, and a logic high (inverted by U58A) is placed on pin 10 of gate U59B which will enable the gate and output a .25 Hz ⊕ 1 Hz clock at U59B pin 8. When

the RESOLUTION/BLANKING switch is set to any position other than 1 Hz, the 10 kHz control signal is dropped (placed at a logic high) and the 2.5 Hz ⊕ 10 Hz clock is enabled by gate U59B.

To summerize the time base functions into a basic logical statement, it is stated that the time base logic exclusively OR selects a 4 second, 1 second, 400 millisecond or 100 millisecond count gate ($\overline{\text{CLOCK}}$) generation by front panel switch action. This statement is expressed by the following Boolean equations, which relates the front panel switch actions to the count gate period (clock frequency).

(RANGE 2) . (1 Hz) = 4 s (.25 Hz)
(RANGE 2) . (1 Hz) = 400 ms (2.5 Hz)
(RANGE 2) . (1 Hz) = 1 s (1 Hz)
(RANGE 2) . (1 Hz) = 100 ms (10 Hz)

CONTROL LOGIC (FIGURE 6-3)
The Control Logic performs command and gating control of the instruments, Count/Display cycles and generates reset pulses allow recycling of the counter. It receives a $\overline{\text{CLOCK}}$ signal from the Time Base Logic which is a count gate of 100 ms, 400 ms, 1 s or 4 s in duration which determines the count cycle period. Front panel inputs consisting of the DISPLAY TIME control, a variable 0 to 1 Meg ohm or open circuit (when placed in the infinite indent) that controls the display time duration, and the MANUAL $\overline{\text{RESET}}$ control from the RESET push button switch (A4S4) which will reset the counter circuits. A NEG INHIBIT and POS INHIBIT command is provided (used with Option P operation only) which will inhibit the counter's entry into the display cycle and prevent outputting of BCD measurement data to a remote device.

The output commands and control signals generated by the Control Logic are listed and defined as follows.

$\overline{\text{GATE}}$; as negative gate of 100 ms, 400 ms, 1s or 4 s duration which controls the count on time of the instrument.

$\overline{\text{STORE}}$; a negative 100 ns to 10 s gate which occurs at the start of the display cycle and will retain the measurement data at the outputs of the storage registers allowing the display of the data.

RESET; a positive 5 μs pulse which will reset certain instrument function allowing the counter to recycle and re-enter the count cycle on the presence of a CLOCK signal.

$\overline{\text{RESET}}$; a negative 5 μs pulse which will reset certain logic functions allowing the counter to recycle and re-enter the count cycle on the presence of a $\overline{\text{CLOCK}}$ signal.

$\overline{\text{PRINT COMMAND}}$; a 650 μs positive pulse that goes high at the start of the display cycle. It informs the remote device that the measurement data has been latched at the storage register and is present at the BCD DATA OUTPUT connector (A5J1) for read out (a Option P function only).

The following detailed circuit analysis is referenced to Figure 6-3 Control Logic Schematic (D-11-05982) and Figure 3-11 Control Logic Functional Logic and Timing Diagram.

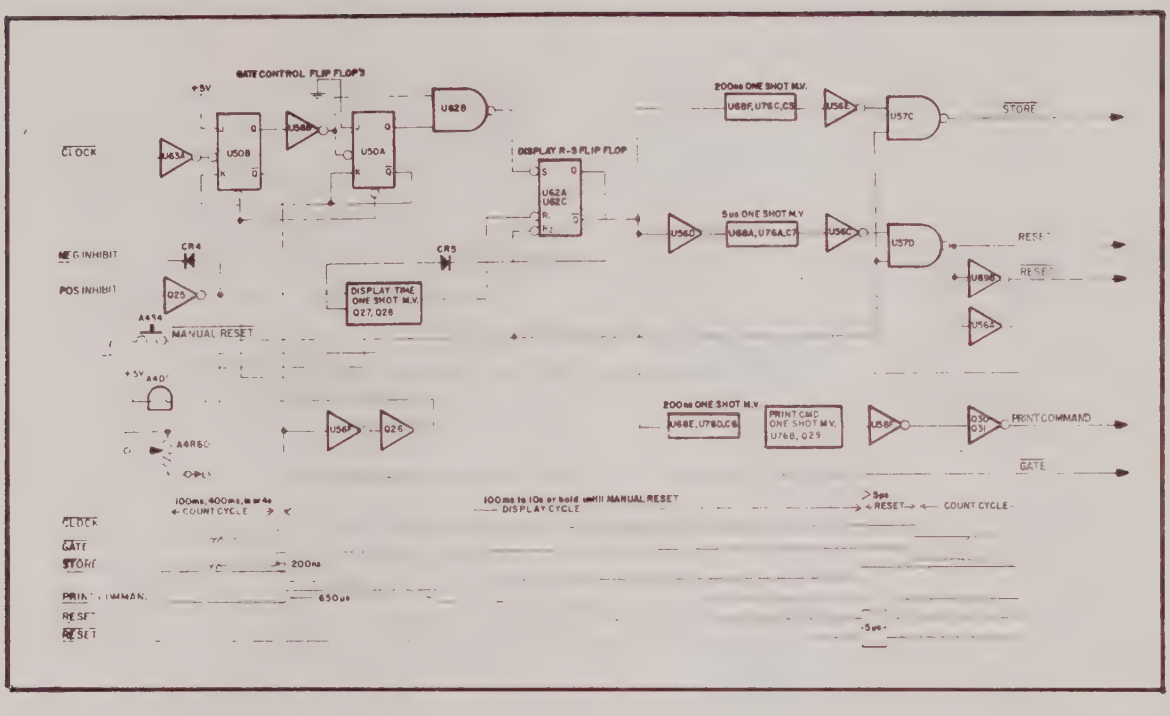


FIGURE 3-11

CONTROL LOGIC FUNCTIONAL LOGIC AND TIMING DIAGRAM

The input $\overline{\text{CLOCK}}$ signal from the Time Base Logic (U59 pin 8) is applied to NOR gate element U63A which is configured as a inverter. U63A inverts the $\overline{\text{CLOCK}}$ signal and applies it to the clock input pin of J-K flip-flop U50B. Because the J input is placed at a logic high at all times a positive gate will be seen at the Q output and a negative gate at the $\overline{Q}$ output. This negative gate at U50B $\overline{Q}$ output is outputted as the GATE signal. The GATE signal is also applied to U56F which inverts it to a logic high and couples it to the base of the lamp driver transistor Q26 which turns on the transistor and provides a 10 ohm return to ground to illuminate the GATE lamp (A4DS1) during count gate on time.

The positive gate at U50B Q output is inverted to a logic low and applied to the clock input of flip-flop Q50A. The J input is returned to ground thus a low will be outputted at the Q output and a high gate is outputted at the $\overline{Q}$ output. The logic high $\overline{Q}$ output is coupled to the K inputs of both GATE CONTROL flip-flops thus effecting a latch to prevent any further $\overline{\text{CLOCK}}$ signals from toggling the CONTROL flip-flops until a reset is generated.

The logic low gate at the clock input of U50A is NAND gated with the logic low gate at U50A Q output and results in a logic high at NAND gate U62B output. At the end of the count-cycle this gate drops to a low and sets the display R-S flip-flop (configured from cross coupled NAND gates U62A and U62C) causing logic high to be set at its Q output and a logic low at its $\overline{Q}$ output. The $\overline{Q}$ output (U62C pin 8) triggers a 200 ns one shot M.V. (U68F, U76C and C5) generating a 200 ns

delay which is inverted by inverter element U56E to a logic high gate that is applied to NAND gate U57C. The other input to U57C is normally pulled up to +5 volts and thus outputs a negative 100ms to 10 s gate which is the $\overline{\text{STORE}}$ command. The $\overline{Q}$ output of the display R-S flip-flop also triggers another 200 ns one shot M.V. (U68E, U76D and C6) which will effect a 200 ns delay and then trigger the print command 650 μs one shot M.V. (U76B, Q29 and its RC circuit components). This one shot M.V. generates a 650 μs gate which is inverted by U58F and then outputted by a push-pull amplifier/driver circuit (Q30 and Q31) as a positive 650 μs duration PRINT COMMAND pulse.

The Q output of the display R-S flip-flop is coupled by diode CR5 as a logic high at set time to the display time one shot M.V. (Q27 and Q28) and will trigger the M.V. if the POS or NEG INHIBIT signals are not active. The display time M.V. will output a gate of 100 ms to 10 s in duration that is set by the front panel DISPLAY TIME potentiometer (A4R60). At the end of this gate which is the termination of the display cycle the signal will go low and reset the display R-S flip-flop, and cause its $\overline{Q}$ output to change state to a high. This action will trigger the 5 μs one shot M.V. (U68A, U76A and C7) which generates a 5 μs gate that is inverted by U56C to a logic low which disables NAND gate U57D and thus generates a 5 μs RESET pulse at U57D's output. The RESET pulse is inverted by logic element U69B and outputted as the RESET signal. A manual reset can be initiated at any time by operator intervention by pressing the push button RESET switch (A4S4), which will place a logic low on U57D pin 13 thus generating a RESET signal, the display R-S flip-flop will also be reset by a logic low being set on U62C pin 10. When a RESET signal is generated automatically or by push button operator action, it is inverted by U56A to a logic low and applied to the gate control flip-flops (U50B and U50A) which resets the flip-flops and allows the counter to re-enter a count cycle on the next CLOCK input gate.

COUNT CHAIN (FIGURE 6-4)

The Count Chain receives its input count in the form of a 1-2-4-8 BCD and a carry from the first DCU located in assembly A1A2. The count/display cycle of the count chain is controlled by the $\overline{\text{STORE}}$ command and the RESET pulse from the control logic. At the end of the count period the $\overline{\text{STORE}}$ command will latch up the eleven counter/Latches U35 thru U34 allowing the measurement data to be displayed. At the termination of the $\overline{\text{STORE}}$ command a 5 μs RESET pulse resets the count chains DCU's U13 thru U22 allowing the chain to reset to zero and re-enter a count period.

A 1-2-4-8 gated BCD count is inputted to the A2 assembly PCB on pads 19, 17, 16 and 18 and applied to the count select gating configuration consisting of IC's U12, U23, U24 and U36 which will AND/OR gate select the input count to the 10^0 or 10^1 counter/Latches (U35 or U47). The count carry (called out as CLOCK on the schematic) is inputted via a coax cable from assembly A1A2 to pad 8 of PCB A2, and then is routed to the carry BCD counter U13 pin 8.

When the front panel's RESOLUTION/BLANKING switch (A4S3) is placed in the 1 Hz position the $\overline{1\ \text{SEC}}$ command at A2 pad 9 is placed at a logic low. This switch selection will select a 1 second time base (range 1 and 3 operation) or 4 second time base (range 2 operation) and configure the count chain for 1 Hz display resolution, allowing all eleven digits to be displayed. When the $\overline{1\ \text{SEC}}$ command is low, control select gates U12B, U23B, U12A and U23A will route the 1-2-4-8 BCD input count to the 10^0 counter/Latch U35. The count carry converted to a 10^1 and 10^2 1-2-4-8 BCD by DCU's U13 and U14 is gated by the select gates U24, U25, U36 and U37 to the 10^1 and 10^2 counter/latches U47 and U48. The 10^2 bit "8" is carried via select gate U49B and inverter U4F to the 10^3 DCU clock input (U15 pin 8). The 10^3 thru 10^{10} DCU's (U15 thru

U22 are cascaded, and output BCD data to their related counter/latches (U26 thru U34).

When the front panel's RESOLUTION/ BLANKING switch is placed in the 10 Hz, 100 Hz, 1 kHz, or 10 kHz position a 100 millisecond time base (range 1 and range 3 operation) or a 400 millisecond time base (range 2 operation) is selected, and the 1 SEC command is placed at a logic high. Control select gates U12B, 23B, U12A and U23A are disabled and select gates U24B, U36B, U24A and U36A will route the input 1-2-4-8 BCD count to the 10^1 counter/latch U47. The BCD output count from DCU U13 is gated to the 10^2 counter/latch U48 via select gates U25B, U37B, U25A and U37A, and the carry bit from U13 pin 12 is routed via select gate U49B and inverter U4F to the 10^3 DCU U15. Logic gating functions of the Strobe Display Logic will provide blanking of the least significant digits in order to relate the visual display with the selected resolution.

The 10^3 thru 10^7 DCU's and their related counter/latches are cascaded by connecting the carry (bit "8") at pin 12 of the DCU to the clock input (pin 8) of the following DCU. The carry from the 10^7 DCU (U19 pin 12) is outputted to the "N" Preset Logic located in assembly A1A4. When the instrument is configured for range 1 or range 2 operation by front panel RANGE switch selection the 10^7 carry is returned by exclusive OR gating logic to the Count Chain and applied to the clock input of the 10^8 DCU at U20 pin 8, thus allowing direct counting of the measurement data. When the instrument is configured for range 3 (auto het) operation a "N" preset count number is supplied by exclusive OR gating of the "N" Preset Logic to the clock input of the 10^8 DCU (U20 pin). This "N" Preset number will preset the 10^8, 10^9, and 10^{10} display digits (the three MSD of the counter to the "N" number. After the "N" number is preset the IF frequency will be counted and displayed by the 10^0 thru 10^7 DCU elements of the count chain, thus providing a direct counter reading of range 3 signal frequency.

STROBE DISPLAY LOGIC (FIGURE 6-5)
The Strobe Display Logic provides the following functional operations.

1. Decodes the 44-line 11 digit 1-2-4-8 BCD measurement data from the count chain into a 10-line multiplexed decimal display drive.

2. Generates a 10 kHz 11-line strobe field to illuminate the display tubes.

3. Provides blanking of up to four of the least significant digits of the display, in order to relate the display to the selected resolution as selected by the front panel RESOLUTION/BLANKING selector switch.

The following detailed analysis is referenced to Figure 6-5 Strobed Display Schematic (D-11-10123) which is located in section 6 of this manual.

Measurement data from the Count Chain is applied via 44-lines to 44 data select NAND gates, which are configured from the eleven IC type SN7403 quadruple 2-input NAND gates (U46 and U54 thru U63). Each quad NAND gate provides a gating element for one of the eleven digits of the display and are enabled by the eleven outputs from the Strobe generator via the eleven inverters (U1 thru U3 elements F and U4 thru 11 elements A). The gate outputs are "OR" wired to form a four wire 1-2-4-8 BCD multiplexed data signal. This output is pulled up to +5 Volts by four 3.3 k ohm resistors (required because the select gates have open collector outputs), and applied to IC type SN74141 (U80). IC U80 which is a BCD-to-Decimal Decoder/Driver, decodes the four line BCD data to a ten line decimal drive which will illuminate the proper decimals of the eleven decimal display tubes (V1 thru V11).

The strobe generator provides eleven sequential 20 microsecond strobes at a 10 kHz rate which

will illuminate the display tubes in a sequential order (MSD to the LSD), and gate on the data select gates in synchronization. A 10 kHz clock signal from the Time Base Logic is applied via PCB A2 pad 29 to pins 3 and 4 of IC U74 which is a type SN74121 monostable multivibrator. This one shot multivibrator triggers on the down clock of the 10 kHz signal and outputs a 20 μ second positive gate at its Q output (U74 pin 6). The gate duration is determined by the externally connected R-C components connected between pins 5, 10, 11, and 14 of U74. This 20 μ second gate is applied to IC element U72B which is the strobe enable gate. The 10 kHz clock signal is also applied to IC U53 a type SN 7493 which is configured as a BCD binary counter and outputs a 1-2-4-8 BCD count to the inputs of a IC type SN7442 a 4-line-to-10-line (1 of 10) decoder (U61). This IC U61 provides full decoding of any valid 4-line BCD input and will ensure that all output remain off for any invalid input condition. The one of ten output provides a logic low true which is inverted to a logic high by its associated inverter and is applied to its related data select gate (U54 thru U63). The sequential order which the strobes are generated in is illustrated by the following truth table.

BCD INPUT		DECIMAL OUTPUT	DISPLAY STROBE
ABCD	DEC	IC OUTPUT	
0000	0	U61-1	10^{10}
1000	1	U61-2	10^{9}
0100	2	U61-3	10^{8}
1100	3	U61-4	10^{7}
0010	4	U61-5	10^{6}
1010	5	U61-6	10^{5}
0110	6	U61-7	10^{4}
1110	7	U61-9	10^{3}
0001	8	U61-10	10^{2}
1001	9	U61-11	10^{1}
0101	10	U72-3	10^{0}
1101	11	U66-6	RESET

NAND gate U72A generates the 10^0 strobe by gating BCD bits "B" and "D" ("2" and "8") which equals decimal 10. Gate U66A generates the strobe sequence reset pulse by NAND gating BCD bits A, B and D ("1", "2" and "8") which is equivalent to decimal 11. The reset pulse outputted at U66 pin 6 is applied to the blanking control flip-flop (U72 pin 9), and to a pulse stretcher U52C and its 650 pFd timing capacitor which lenghtens and inverts the pulse to reset the BCD binary counter U53 at the end of a strobe count sequence.

The digit blanking function is provided by the front panels RESOLUTION/BLANKING switch (A4S3) selection of the 10^0, 10^1, 10^2, or 10^3 digit strobe as the trigger source of the blanking R-S flip-flop (configured by the cross-coupled gates U72D and U72C). When the switch (A4S3) is placed in the 10 Hz position the 10^0 strobe is selected as a logic low via PCB pad AB, the switch contact, and PCB pad AA and applied to U72 pin 13, which toggles the flip-flop placing a logic low at U72 pin 8. This logic low will disable the strobe enable gate U72B at 10^0 strobe on time, and in turn effect a disable of the strobe output gates until a strobe reset pulse is generated that resets the blanking control flip-flop thus re-enabling the strobe output gates. The above described action blanks the display from 10^0 strobe on-time to the strobe sequence reset time and prevents the least significant digit (units) from being displayed. When the switch is placed in the 100 Hz position the 10^1 strobe is selected via PCB pad AC and will provide blanking from the 10^1 strobe on time to strobe sequence reset time thus effecting a blanking of the two least significant digits (units and tens). The selection of the 1 kHz or 10 kHz switch position will effect the blanking of the three or four least significant digits, in the same manner as the other blanking selections, thus providing blanking of the unit thru hundred or unit thru thousand display tubes.

The digit strobe drive is provided by the eleven 2N5833 type transistors (Q1 thru Q11), which when turned on by the appropriate strobe output gate, will place a low on the base of the

related digit control transistor (Q12 thru Q22) and apply +190 Volts to the anode of the selected display tube (V1 thru V11) for a 20 microsecond period.

3.3.19 POWER SUPPLY ASSEMBLY A3 (FIGURE 6-19)

The Power Supply Assembly is contained on a separate PCB designated A3 and contains the rectifier diodes, IC voltage regulators and filter capacitors. The power transformer (A5T1) is mounted on the rear panel and its secondary windings are hard wired to the PCB pads. Paragraph 3.2.4 on page 3-7 details the ac power distribution and Table 3-3 also located on page 3-7 lists the dc output voltages, their functions and the A3 PCB pad numbers of the output voltage connections.

The power supply has no adjustments, does not use any zener diodes for voltage reference and contains no precision resistor voltage divider networks to provide reference voltages. The regulation of all the regulated outputs is performed by IC monolithic voltage regulators. The voltage regulators are essentially "blow out" proof being self limiting in nature. In addition these devices are provided with a thermal shutdown feature to prevent the IC from overheating. If the device internal thermal dissipation becomes too great the regulators will switch on and off at a duty cycle that will prevent excessive overheating. If a intermittent output condition is noted as a malfunction, the problem most likely is the load and not the regulator. The voltage regulators meet worst case output conditions, including variations in temperature, input voltage, load and long term stability, and are well within the operating range of the digital logic that they supply.

Two unregulated outputs are provided, a +190 volts for the display tube anodes, and a +28 volts which supplies the YIG oven heater element. Diode CR7 provides half-wave rectification for the +190 volt supply and R1, R3 and C5 make up the filter network. The +28 volt unregulated output is supplied by full-wave rectifier CR8 and CR9 and filtered by C4. This full-wave rectifier also supplies a raw 30 volts which is prefiltered by C3 and C14 and applied to the +18 volt IC regulator U5, its regulated output is filtered by C13 and outputted via pad 13 to the YIG tuning coil. The positive and negative 12 volt regulators U3 and U2 are supplied by a bridge rectifier comprised of CR1 thru CR4 and output regulated +12 volts at pads 9 and 10, and -12 volts at pads 5 and 8 to the linear IC's located in the auto het assembly A1 that require 12 volts for V_{cc} and V_{ee}. The 5 volt rectifier CR10 thru CR13 supplies raw +5 volts via pad U and its ground return pad T to the Clock Control Assembly A5A1 which contains an internal +5 volt IC voltage regulator (A5A1U1). Regulator U4 provides regulation for the +5 volts that supplies the V_{cc} to the auto het section A1 via pad 11. The other +5 volt regulator U7 supplies V_{cc} regulated +5 volts to the Counter Assembly A2 via pads 20 and 21. IC U6 is a -5.2 voltage regulator and supplies -5.2 volts Vee to ECL logic located in assembly A1 via pads 18 and 19.

The circuitry noted as "E" option on figure 6-13 is located on the power supply assembly A3, and is a optional +28 volt regulated power supply supported by transformer T2 which is provided when E option, a reference oscillator assembly of greater stability is installed. Refer to Section 7 of this manual for the E option information if required.

SECTION 4

MAINTENANCE AND CALIBRATION

SECTION 4

MAINTENANCE AND CALIBRATION

4.1 INTRODUCTION

Section 4 presents pertinent information to maintain the Model 988/989 Microwave Frequency Counter. The section is divided into three subsections which cover Normal (routine) Maintenance, Calibration and Alignment, and Troubleshooting and Repair Techniques. Table 4-1 offers a list of recommended test equipment required for instrument calibration, alignment and troubleshooting.

TABLE 4-1

RECOMMENDED TEST EQUIPMENT

INSTRUMENT DESCRIPTION	MANUFACTURER AND MODEL	MINIMUM REQUIREMENTS
Frequency Standard	HP 105A/B	10 times internal oscillator accuracy.
Oscilloscope	Tektronix 454A	150 MHz bandwidth, Dual trace.
Digital Voltmeter	Eldorado Model 1810	1% accuracy
Spectrum Analyzer	Tektronix 7L12 Plug in using TEK 7603 main frame	100 kHz to 1.8 GHz
Sweep Oscillator	HP 86200 series w/86220A plug in	0 to 200 MHz ±1%
LF Signal Generator	HP 202C	Combined range from 20 Hz to 18 GHz
HF Signal Generator	HP 606A	
VHF Signal Generator	HP 608C	
UHF Signal Generator	HP 612A	
UHF Signal Generator	HP 614A	

Table 4-1 Recommended Test Equipment (continued)

UHF Signal Generator	HP 616B	Combined range from 20 Hz to 18 GHz
SHF Signal Generator	HP 618C	
SHF Signal Generator	HP 620B	
SHF Signal Generator	HP 626A	
SHF Signal Generator	HP 628A	
Frequency Counter	Eldorado Model 1460	0 to 200 MHz Counter with totalizer function.
D/A Converter test fixture	Eldorado 988/989 D/A Converter test fixture	

4.2 ROUTINE MAINTENANCE

Routine or periodic maintenance (PM) is the systematic servicing and inspection of an electronic instrument to prevent occurance of a fault or failure. The severity of the operating environment normally determines the frequency of the maintenance periods.

4.2.1. Instrument Cleaning

Cleaning of the instrument is done on a as required basis, as the frequency of the cleaning routine is dependent on the operating environment. Clean the instrument by brushing, wiping with a lint free cloth, vacuuming or blowing with low pressure compressed air ($\leq$30 PSI). Solvents (non-corrosive) may be used if additional cleaning action is necessary. The following materials, or their equivalents are recommended for use.

1. Lint free cloth or disposable wipers.
2. Solvent (alcohol/water 50/50).
3. Compressed air (filtered, moisture-and-oil free, 30 psi maximum).

4.2.2. Preventative Maintenance Checks

Perform the following checks monthly or as deemed appropriate with environmental operating conditions.

1. Check the tightness and condition of all the internal connectors.
2. Operate the instrument in the TEST mode and observe that the mechanical action of all switches and controls, is smooth and free of binding, no looseness of their mounting is apparent and no play is present with proper dedent setting thus allowing proper resetability.
3. Check the 1 MHz output with reference to a frequency standard .

Perform the following maintenance checks on

a quarterly basis or as deemed appropriate.

1. Check power transformer and power supply components; Inspect the wiring on the power transformer for signs of overheating, inspect filter capacitors for dirt, corrosion or oil and clean or replace as required.
2. Inspect all internal components for physical integrity.
3. Inspect cables and wires for chaffed, cracked, or frayed insulation.
4. Perform the incoming inspection check as outlined in Section 2.2.

4.3 CALIBRATION AND ADJUSTMENT PROCEDURES

4.3.1
The periodic adjustment of the internal oscillator assembly A7 frequency is the only routine calibration requirement of the Model 988/989 Microwave Frequency Counters. The other internal adjustments, are originally set at the factory during final test and alignment and are not subject to periodic adjustments, these adjustments can be considered as "semi-fixed" and their alignment is necessitated only when certain components are replaced or a out-of-tolerance condition in the performance specification is noted.

4.3.2 Internal Reference Oscillator Calibration

The frequency of the internal reference oscillator is adjusted relative to a 1 MHz frequency standard. Figure 4-1 illustrates the reference oscillator standardization configuration and adjustment location, and Table 4-2 provides the step-by-step procedure that is required to perform the reference oscillator standardization. A frequency standard having ten times the stability of the Model 988/989 internal reference oscillator is required.

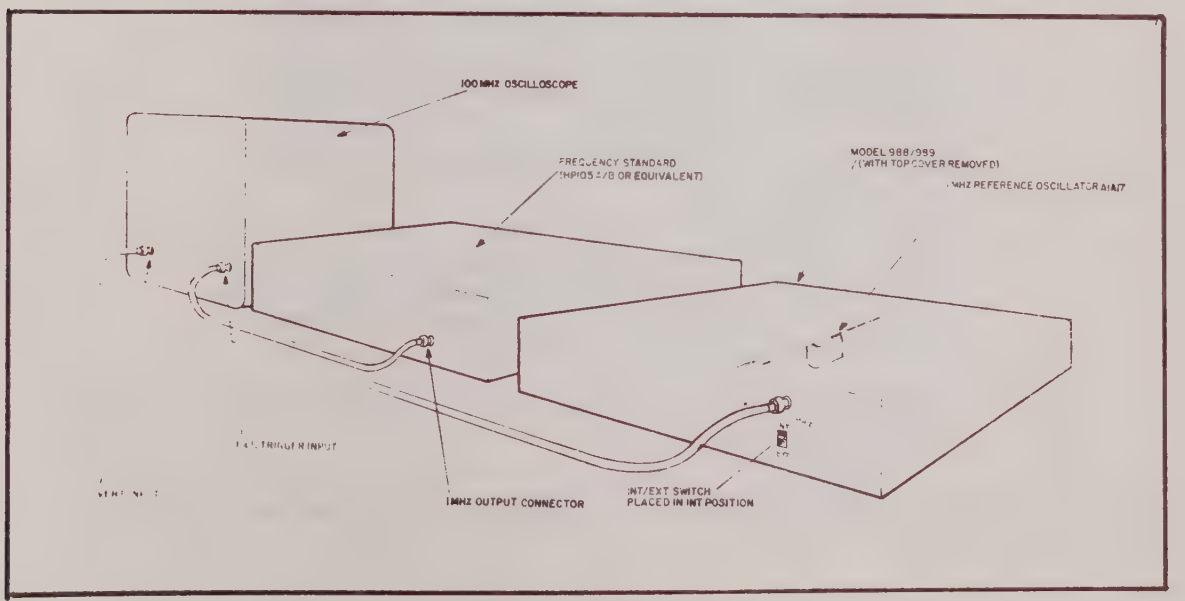


FIGURE 4-1

INTERNAL OSCILLATOR STANDARDIZATION CONFIGURATION

TABLE 4-2

1 MHz REFERENCE OSCILLATOR STANDARDIZATION PROCEDURE

STEP	ACTION
1	Apply power to the Model 988/989 Microwave Frequency Counter, and allow a minimum of four hours continuous operation for oscillator stabilization.
2	Connect the oscilloscope's vertical input to the Model 988/989 rear panel 1 MHz INT/EXT BNC connector.
3	Insure that the rear panel 1 MHz INT/EXT switch is placed in the INTernal position.
4	Connect the frequency standard's 1 MHz output to the external trigger input of the oscilloscope.
5	Remove the top cover from the Model 988/989 to provide access to the 1 MHz frequency trimmer located on the reference oscillator A7.
6	Place the oscilloscope's TIME/DIV time base switch in the 0.5 μ sec. position (500 ns/DIV), and select external triggering mode.
7	Adjust the oscilloscope's trigger level and vertical conditioning controls to obtain a CRT display, a train of 5 pulses (one pulse per two divisions) will drift or run across the CRT sweep.
8	Adjust the oscillators frequency trimmer for minimum drift of the pulse train.
9	Observe the pulse train for five minutes or longer noting the drift rate. If the drift rate increases readjust, then continue to monitor and trim the frequency adjustment until a minimum drift rate is realized.
10	Disconnect the test configuration and replace the Model 988/989's top cover.

4.3.3 Range 1 Input Amplifier Threshold Adjustment Procedure

If a component is replaced that effects the range 1 input amplifier's sensitivity or the instrument counts in range 1 on input amplifier noise, adjustment of the Range 1 threshold control is required. Table 4-3 provides the step-by-step procedure of the Range 1 Input amplifier threshold adjustment.

TABLE 4-3

RANGE 1 INPUT THRESHOLD ADJUSTMENT PROCEDURE

STEP	ACTION
1	Place the POWER ON/OFF switch in the OFF position, remove the instruments top cover, and extend PCB A1A1 using a extender board (Eldorado P/N 79-10847A) to allow access to control A1A1R4.
2	Reapply power by placing the POWER switch to the ON position. Place the INPUT switch to the RANGE 1 position and the RESOLUTION/BLANKING to the 1 Hz position.
3	With no signal applied to the RANGE 1 INPUT connector adjust the threshold control A1A1R4 for a front panel display reading of 00 000 000 001.
4	Apply a 100 MHz, 50 mV rms (-13dBm) signal generator to the RANGE 1 INPUT BNC connector and verify that the display reads 00 100 000 000.
5	Remove the signal generator input, turn off the instrument by placing the POWER switch in the OFF position, and remove the extender board. Replace the A1A1 PCB assembly in to its connector and replace the top cover of the instrument.

4.3.4 Start Detector Level Adjustment and Range 3 Input Meter Calibration Procedures

If a component is replaced that effects the Range 3 DETECTOR CURRENT level, the Range 3 Input Level Meter reads in error, or the START command is not being generated on the presence of a input signal, perform the procedure provided by Table 4-4. Figure 4-2 supports the procedure as to the adjustments and monitoring test point locations.

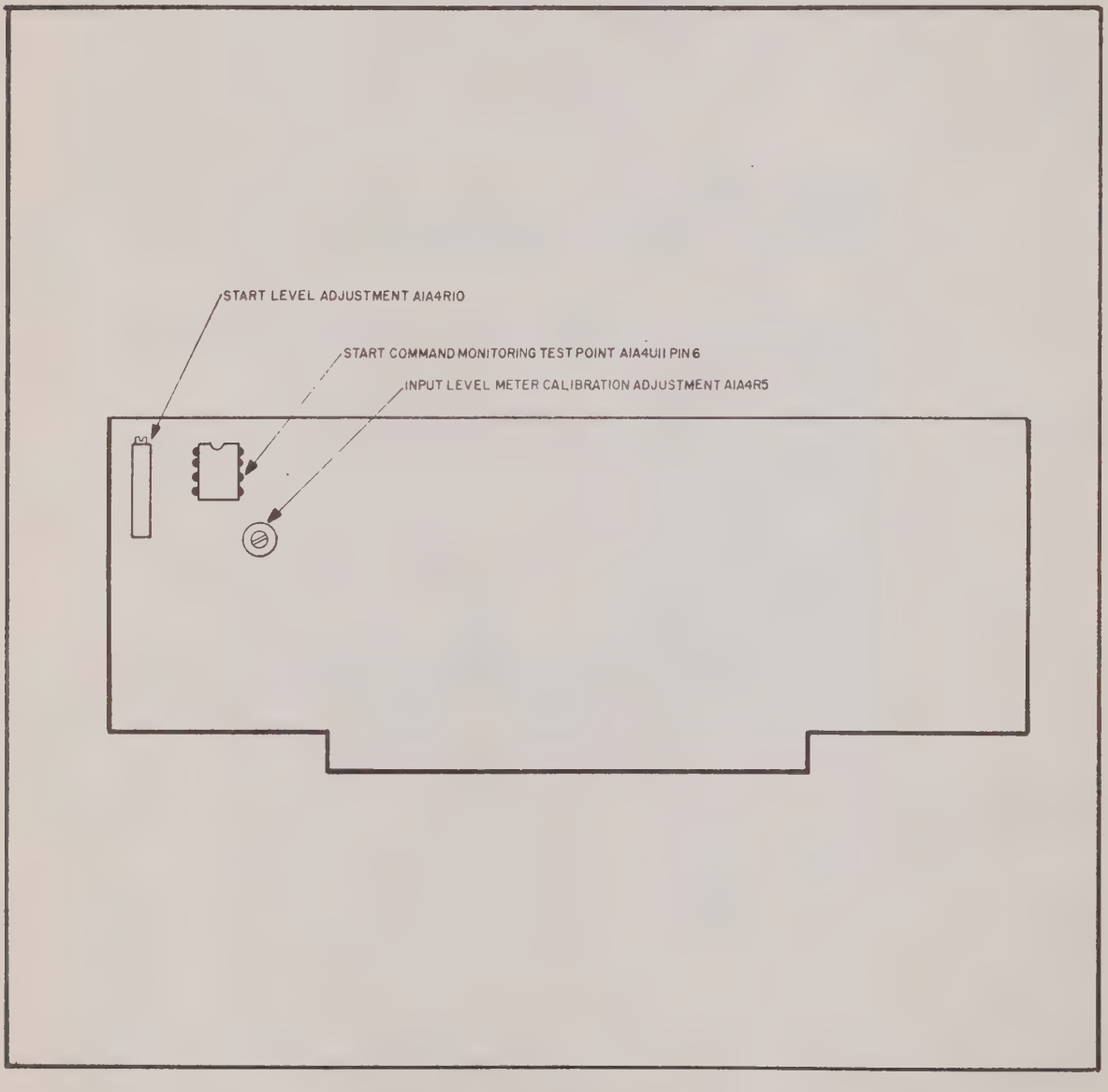

START LEVEL ADJUSTMENT A1A4R10
START COMMAND MONITORING TEST POINT A1A4U11 PIN 6
INPUT LEVEL METER CALIBRATION ADJUSTMENT A1A4R5

FIGURE 4-2

START DETECTOR ADJUSTMENTS AND MONITORING TEST POINT LOCATION DIAGRAM

TABLE 4-4

START DETECTOR LEVEL ADJUSTMENT

AND RANGE 3 INPUT METER CALIBRATION PROCEDURE

STEP	ACTION
1	Place POWER switch in the OFF position, remove instrument's top cover, and extend A1A4 PCB assembly using a extender board (P/N 79-10874A).
2	Reapply power by placing the POWER switch in the ON position and place the INPUT switch in the RANGE 3 position.
3	Verify that the RANGE 3 INPUT LEVEL meter's pointer is set at the center of the white area (1/4 full scale deflection) if not adjust the meter mechanical zero adjustment to place the pointer at the center of the white area.
4	Apply a 3 GHz 0 dBm (200 mV rms) signal from a signal generator to the RANGE 3 INPUT "N" type connector, and adjust the Input Level Meter Calibration adjustment A1A4R5 for a meter indication of half scale deflection, (centered in the green area). Adjust the 3 GHz test signal input level from -7 dbm to + 10 dBm to verify that the meter pointer swings thru the green area on the meter face.
5	Readjust the 3 GHz test signal to a level of -9 dBm. Connect a oscilloscope to pin 6 of IC A1A4U11 to monitor the START command signal.
6	Rotate the Start Level control (A1A4R10) fully CCW, then rotate the control slowly CW while monitoring the oscilloscope until a START command is indicated by a level shift from 0 volts to +5 volts as viewed on the oscilloscope's CRT.
7	Disconnect the test configuration, place the POWER switch to the OFF position, remove extender board, and replace assembly A1A4 in its connector and replace instrument's top cover.

4.3.5 Stop Detector Alignment Procedure

The Stop Detector PCB assembly A1A7 contains three detector circuits which monitor the IF signal and generates STOP command signals when a IF signal is within the proper frequency band and at a level of -70 dBm or greater. If the Stop Detector does not generate STOP command signals on the presence of the proper IF signal or it generates STOP commands on an invalid IF signal the Stop Detector alignment procedure provided in Table 4-5 should be performed. Figure 4-3 illustrates the adjustments and tests point locations on the A1A7 PCB.

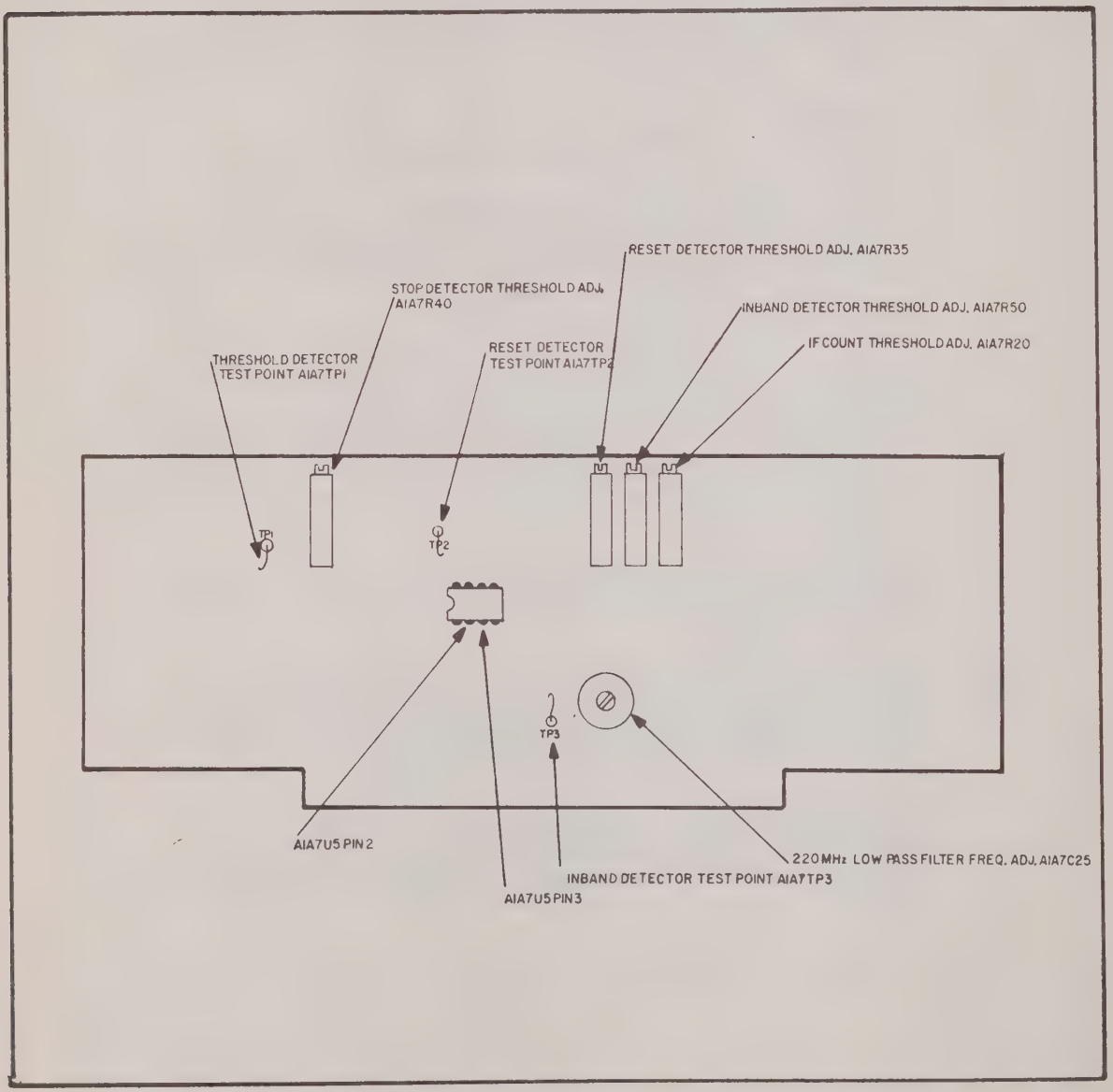

RESET DETECTOR THRESHOLD ADJ. AIA7R35
STOP DETECTOR THRESHOLD ADJ. AIA7R40
INBAND DETECTOR THRESHOLD ADJ. AIA7R50
IF COUNT THRESHOLD ADJ. AIA7R20
THRESHOLD DETECTOR TEST POINT AIA7TP1
RESET DETECTOR TEST POINT AIA7TP2
TP1
TP2
TP3
AIA7U5 PIN 2
AIA7U5 PIN 3
INBAND DETECTOR TEST POINT AIA7TP3
220 MHz LOW PASS FILTER FREQ. ADJ. AIA7C25

FIGURE 4-3

STOP DETECTOR A1A7 ADJUSTMENTS AND TEST POINT LOCATION DIAGRAM

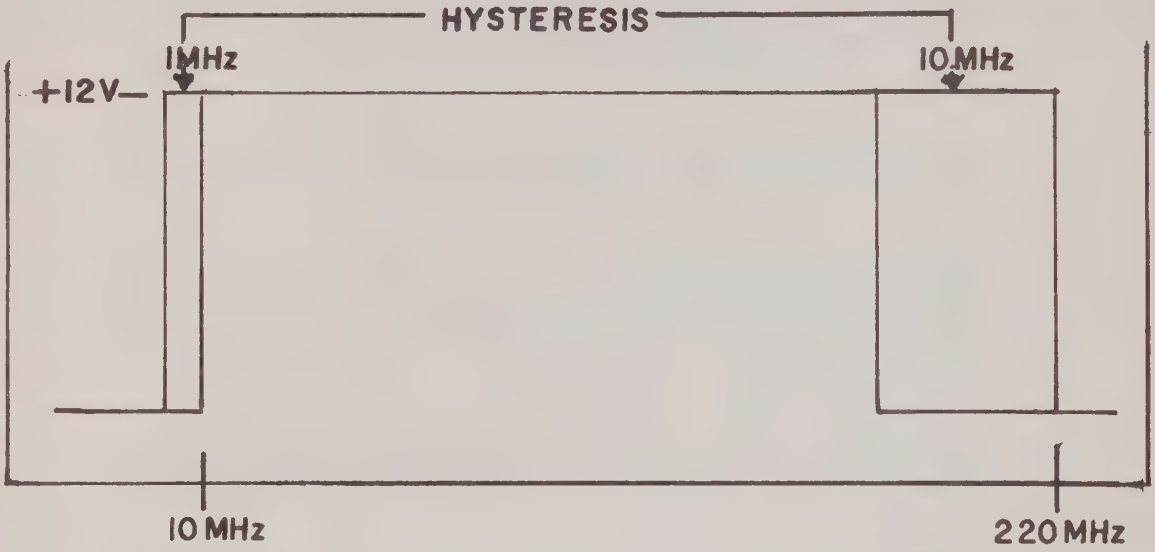
TABLE 4-5

STOP DETECTOR ALIGNMENT PROCEDURE

STEP	ACTION
1	Remove power from instrument by placing the POWER ON/OFF switch in the OFF position. Remove instruments top cover and extend STOP DETECTOR AND IF SHAPER PCB assembly A1A7 with the use of Extender Board (P/N 79-10874A).
2	Disconnect the coax cables from A1A2 PCB assembly connectors A1A2J2 (Range 3 input) and A1A2J3 (Range 1 input). Connect the coax cable that was on A1A2J2 to A1A2J3.
3	Disconnect the coax cable from the IF Amplifier Assembly (A1A13) INPUT connector (A1A13 INPUT) and connect a Sweep Generator 5 MHz to 255 MHz, (HP 86200 series main frame w/86220A plug in) or equivalent, with a 50 ohm coax test cable to the A1A13 INPUT connector.
4	Apply power to the instrument by placing the POWER switch in the ON position, and place the INPUT switch in the RANGE 1 position.
5	Set the Sweep Generator for a 225 MHz signal having a -66 dBm output level. Adjust the IF COUNT THRESHOLD control (A1A7R20) for a front panel display readout of 00 225 000 000 (±1 count).
6	With no signal applied from the Sweep Generator measure the voltage at A1A7U5 pin 2 with a Digital Voltmeter and note its reading. Place the Digital Voltmeter's test probe on A1A7U5 pin 3 and adjust the INBAND DETECTOR THRESHOLD control (A1A7R50) for a voltage level which is 30 mV more negative than the level measured at A1A7U5 pin 2.
7	Connect the Sweep Generators SWEEP OUTPUT ramp signal to the HORIZ. input of a oscilloscope. Connect the oscilloscope's VERT input via a X10 Scope Probe to the INBAND DETECTOR TEST POINT (A1A7TP3). Set up the oscilloscope's horizontal controls for sweep of 10 full division on the CRT. Configure the oscilloscopes vertical controls for a 5 V/Division CRT display. Configure the Sweep Generator's STOP and START controls for a 5 MHz to 250 MHz sweep and set the POWER LEVEL control for a -60 dBm output with RF blanking turned off.

Table 4-5 Stop Detector Alignment Procedure (continued)

8	Adjust the 200 MHz LOW PASS FILTER FREQ. ADJ control (A1A7C25) for a oscilloscope CRT display as illustrated in the figure below :



9	Configure the Sweep Generator for MANUAL mode and manually sweep through 205 MHz to 225 MHz while monitoring the oscilloscope's CRT display. While sweeping upward the signal should go negative between 220 MHz and 225 MHz, and while sweeping downward from 225 MHz to 205 MHz the signal should go positive between 212 MHz to 208 MHz. If the width of the hysteresis does not meet the above conditions it can be corrected by selecting the value of A1A7R51 which has a nominal value of 100 k ohms.
10	Manually sweep from 5 MHz to 15 MHz, the signal should switch to +12 volts between 6 MHz and 11 MHz with the hysteresis being approximately 1 MHz wide.
11	Adjust the Sweep Generator for a 175 MHz signal with a level of -60 dBm. Connect the vertical input of the oscilloscope to the RESET DETECTOR TEST POINT A1A7TP2, and rotate the RESET DETECTOR THRESHOLD control A1A7R35 in a CCW direction until the monitored level goes high (approximately +4 volts), then rotate the control in the CW direction until the signal level just goes low (0 volts).

Table 4-5 Stop Detector Alignment Procedure (continued)

12	Set up the Sweep Generator for a 100 MHz to 250 MHz -60 dBm output, with the RF blanking placed ON. Connect the oscilloscope's probe to the THRESHOLD DETECTOR TEST POINT A1A7TP1. Rotate the STOP DETECTOR THRESHOLD ADJ control A1A7R40 to the CW limit, then rotate it slowly in the CCW direction until a positive pulse, of approximately 3 volts amplitude is present at the start of the oscilloscope's sweep display.
13	Remove power from the instrument by placing the POWER switch in the OFF position. Disconnect the test configuration, remove extender board and replace the A1A7 assembly into its connector. Return all the coax cables to their normal configuration. Do not replace the instruments top cover at this time.
14	Reapply power to the instrument by placing the POWER switch in the ON POSITION, and place the INPUT switch to RANGE 3 position. Apply a 3 GHz -7 dBm (100 mV rms) to the RANGE 3 INPUT "N" type connector, and verify that the counter locks-on and displays 03 000 000 xxx. If the counter does not lock on properly to the input test signal, rotate the STOP DETECTOR THRESHOLD ADJ control (A1A7R40) one revolution in the CCW direction, and re-check for proper lock on.
15	Remove the input test cable and replace the top cover.

4.3.6 Phase Lock Oscillator Adjustments

The output of the Phase Lock Oscillator assembly A1A12 must be 20 MHz and locked in phase with the 1 MHz reference input phase lock clock signal. If a component part of the phase lock oscillator circuit is replaced which can effect the operation or a incorrect display readout in Range 3 measurements is indicated, the 20 MHz phase locked signal should be checked, and if out of phase corrected by adjustment of trimmer capacitor A1A12C5. Table 4-6 provides the procedure for verifying the 20 MHz signal and performing the required adjustments. Figure 4-4 illustrates the test configuration to accomplish this procedure. The Phase Lock Oscillator functions in the Range 3 mode (Auto Het) only and has no effect on the operation of Range 1 or Range 2 counting modes, thus the 20 MHz phase lock signal can be verified by applying it to the Range 1 input and counting and displaying it as a normal Range 1 measurement operation.

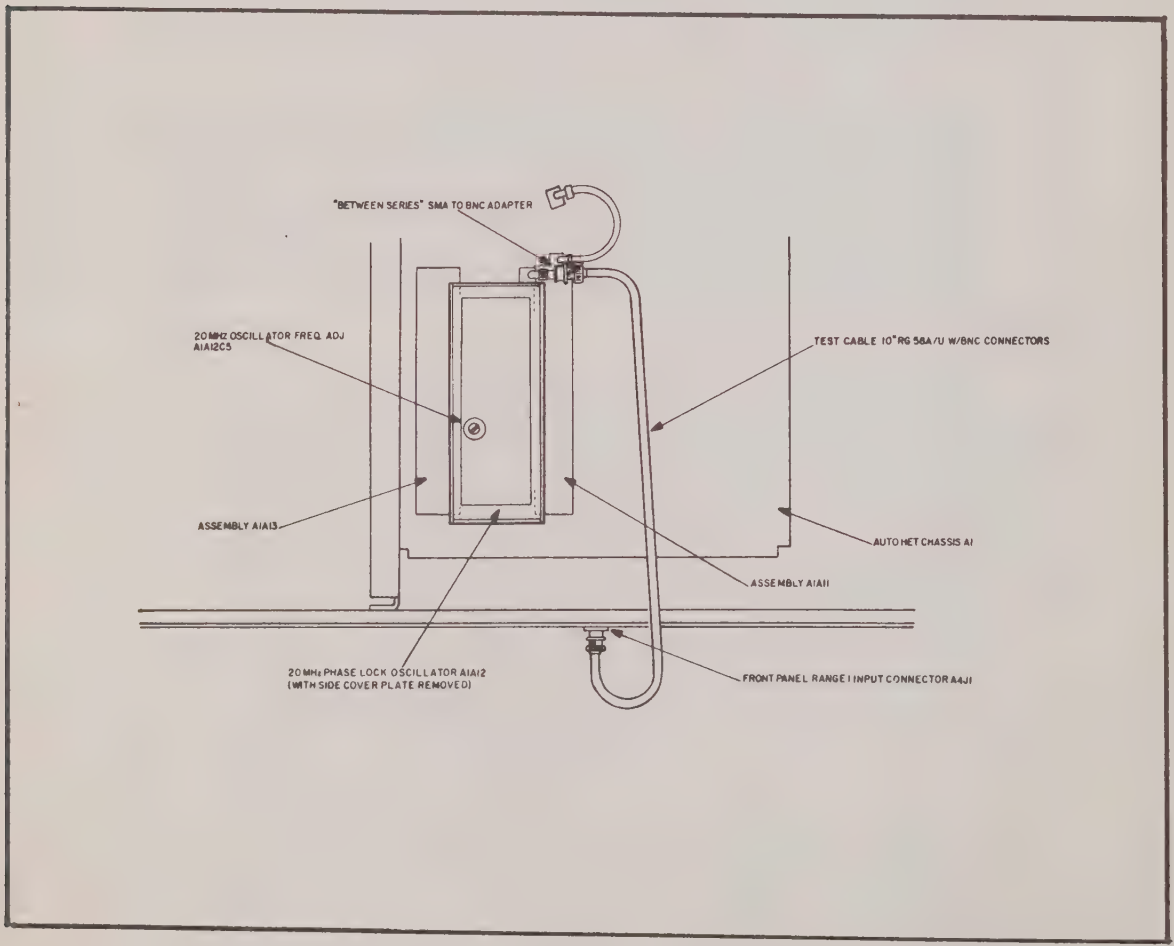

"BETWEEN SERIES" SMA TO BNC ADAPTER
20 MHz OSCILLATOR FREQ. ADJ A1A12C5
TEST CABLE 10" RG 58A/U W/BNC CONNECTORS
ASSEMBLY A1A13
AUTO HET CHASSIS A1
ASSEMBLY A1A11
20 MHz PHASE LOCK OSCILLATOR A1A12 (WITH SIDE COVER PLATE REMOVED)
FRONT PANEL RANGE I INPUT CONNECTOR A4J1

FIGURE 4-4

PHASE LOCK OSCILLATOR TEST CONFIGURATION

TABLE 4-6

20 MHz PHASE LOCK OSCILLATOR ADJUSTMENT PROCEDURE

STEP	ACTION
1	Remove Power from the instrument by placing the POWER OFF/ON switch in the OFF position and remove the top and bottom covers.
2	Disconnect the coax cable from the Phase Lock Oscillator Assembly A1A12's output connector (the output connector is the SMA coax connector mounted on the rear of the assembly).
3	From the bottom of the Auto Het Chassis A1 remove the two 4-40 mounting screws that secure the 20 MHz Phase Lock Oscillator Assembly A1A12 to the chassis.
4	From the top of the instrument lift the A1A12 assembly upward to clear the assemblies located on both of its sides and rotate it CW 90° in the horizontal plane, then place it on top of assemblies A1A11 and A1A13.
5	Remove the side cover plate of the A1A12 assembly to provide access to the 20 MHz Oscillator Frequency Adjustment A1A12C5, located on the component side of the assemblies internally mounted PCB.
6	Connect a 10 inch 50 ohm coax test cable between the A1A12 OUTPUT connector and the front panel mounted RANGE 1 INPUT connector A4J2. A "between series" coax adapater SMA to BNC is required to configure the cable to the A1A12 OUTPUT connector.
7	Apply power to the instrument by placing the POWER switch in the ON position, and place the INPUT switch in the RANGE 1 position.
8	Monitor the instruments front panel display for a readout of 00 020 000 000 (± 1 count). If the display does not indicate 20 MHz (±1 Hz), adjust trimmer capacitor A1A12C5 for a correct readout on the display. Monitor the display for a number of count cycles to insure that the 20 MHz Phase Lock Oscillator remains locked on at 20 MHz with the 1 MHz Reference Oscillator.

Tabel 4-6 20 MHz Phase Lock Oscillator Adjustment Procedure (Continued)

9	Remove power from the instrument and replace the side cover plate of assembly A1A12, and reinstall the assembly by using the reverse sequence from which it was removed.
10	With the test cable still connected from the 20 MHz Oscillator output to the front panel's Range 1 input, reapply power to the instrument and verify that the 20 MHz Oscillator is on frequency and phase locked by noting the display readout is indicating 20 MHz (± 1 Hz).
11	Remove power from the instrument, disconnect the test configuration, replace the coax cable connection between assemblies A1A12 and A1A11, and replace the top and bottom covers of the instrument.

4.3.7 200 MHz Frequency Multiplier Alignment.

The 200 MHz Frequency Multiplier Assembly A1A11 multiplies the 20 MHz Signal from the Phase Lock Oscillator Assembly A1A12 to 200 MHz and outputs to the 200 MHz Power Amplifier Assembly A1A9. The output signal must be 200 MHz at a level of + 12 dBm to + 18 dBm with side band rejection of the 20 MHz harmonics of at least - 65 dBm. If a Auto Het operation malfunction indicates a 200 MHz Multiplier fault, or a component has been replaced that effects the 200 MHz Multipliers operation, perform the alignment procedure in Table 4-7. Figure 4-5A illustrates the adjustment holes drill out locations and the adjustment callouts. Figure 4-5B illustrates a Spectrum Analyzer display on a Tektronix 7L12 plug-in Spectrum Analyzer with a 7000 series oscilloscope main frame.

FIGURE 4-5A
200 MHZ FREQUENCY MULTIPLIER ASSEMBLY A1A11
COVER PLATE WITH ADJUSTMENT ACCESS HOLES
DRILLING LOCATION AND ADJUSTMENT CALLOUTS

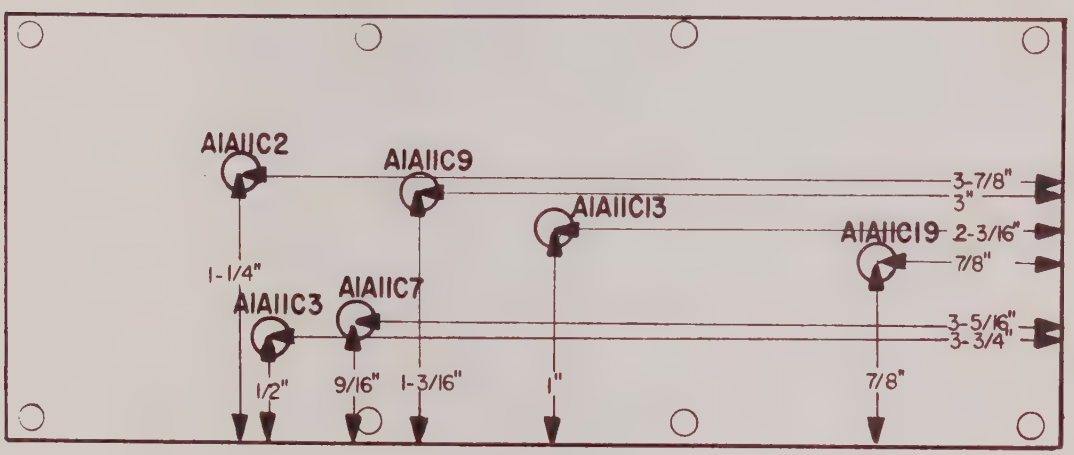


FIGURE 4-5B
200 MHZ FREQUENCY MULTIPLIER OUTPUT SPECTRUM

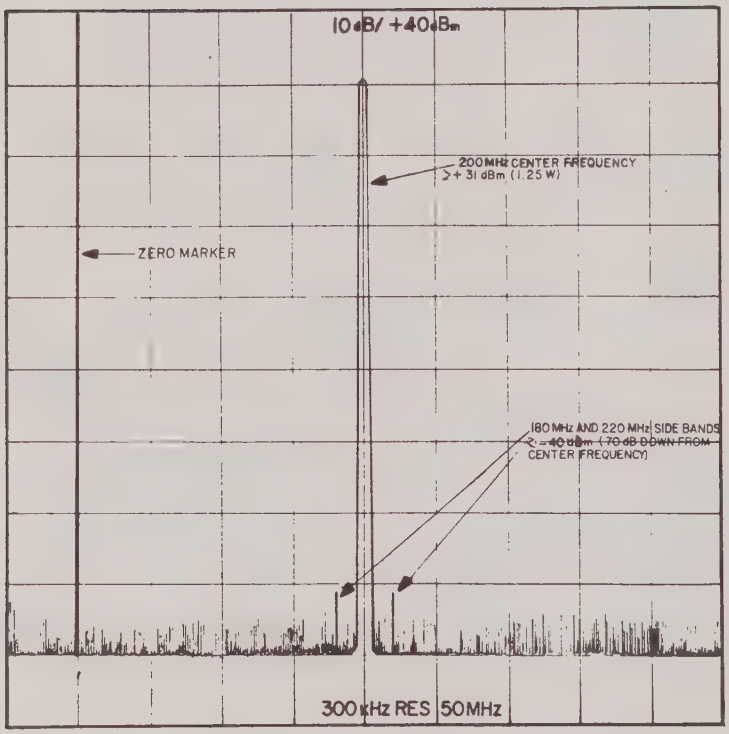


TABLE 4-7

200 MHZ FREQUENCY MULTIPLIER ADJUSTMENT PROCEDURE

STEP	ACTION
1	Verify that the Phase Lock Oscillator A1A12 is providing the proper 20 MHz drive by monitoring the signal with a Spectrum Analyzer (TEK 7L12 w/7000 series main frame or equivelent) at A1A12 OUTPUT Connector. This signal must be 20 MHz and referenced to the 1 MHz Reference Oscillator and have a level of + 1 dBm to + 3 dBm.
2	Monitor the output of the 200 MHz Frequency Multiplier A1A12 with a Spectrum Analyzer to verify that its output is actually out of the required parameters. The signal must be 200 MHz with a level of + 12 dBm to + 18 dBm and all of its harmonics must be less than - 65 dBm. When monitoring the spectrum for its spectral purity pay special attention to the 180 MHz and 220 MHz side bands, refer to Figure 4-5B which provides a illustration of a proper 200 MHz Frequency Multiplier output spectrum. If the output meets the above stated parameters do not attempt to adjust the 200 MHz Frequency Multiplier for improved side band rejection. On the other hand if the output is out of its required parameter proceed to step 3.
3	From the bottom of the Auto Het Chassis A1 remove the two 4-40 mounting screws that secure the 200 MHz Frequency Multiplier Assembly A1A11 to the chassis.
4	From the top of the instrument lift the A1A11 assembly upward to clear the assemblies located on both of its sides and rotate CW 90^0 in the horizontal plane, then place it on top of assemblies A1A9 and A1A12.
5	Remove the side cover plate from the A1A11 assembly and drill six 5/32" holes to provide adjustment access to the PCB mounted trimmer capacitors, refer to Figure 4-5A for the drilling center locations.
6	Dress the drilled holes to remove any burrs, and replace the cover plate on the assembly securing it with the eight 2-56 mounting screws.
7	Refer to Figure 6-16 the 200 MHz Frequency Multiplier Schematic Diagram making note of the following listed trimmer capacitors and their circuit relationship. 1. A1A11C3 Times five multiplier adjustment; provides for the adjustment of A1A11Q1 collector tuned circuit to 100 MHz. 2. A1A11C13 Times two multiplier adjustment; provides for the adjustment of A1A11Q2 collector tuned circuit to 200 MHz.

TABLE 4-7

200 MHZ FREQUENCY MULTIPLIER ADJUSTMENT PROCEDURE

Continued

STEP	ACTION
	3. A1A11C19 Output coupling circuit; provides for the adjustment of the frequency of the output tank circuit. 4. A1A11C2 Input coupling circuit adjustment; provides for the adjustment of A1A11Q1 base tuned circuit. 5. A1A11C7 Times five multiplier output coupling circuit frequency adjustment. 6. A1A11C9 Times two multiplier input coupling circuit frequency adjustment.
8	Using a non-metallic alignment tool alternately adjust A1A11C3 trimmer capacitors for a 200 MHz output signal, by monitoring the output on the Spectrum Analyzer.
9	With a non-metallic alignment tool alternately trim A1A11C2, C7, C9 and C19 for minimum side bands and a maximum 200 MHz center frequency mode on the Spectrum Analyzer. Figure 4-5B depicts the proper Spectrum Analyzer display.
10	When a output that meets or exceeds the required parameters is obtained remove the assembly cover plate and seal the adjustment access holes that were drilled by taping and screwing in plugs or inserting snap button hole (Butch) plugs.
11	Replace the assembly's cover plate, remount the A1A11 assembly to the Auto Het Chassis and reconnect the coax cable to the assembly's output connector.

4.3.8 200 MHz Power Amplifier Alignment.

200 MHz Power Amplifier Assembly A1A9 amplifies the 200 MHz signal from the 200 MHz Frequency Multiplier Assembly A1A11 and outputs a 1.5 watt drive to the YIG tuned Multiplier A1A8. This YIG drive must be 200 MHz at a level of at least + 30 dBm (1 watt) with the side band rejection of the 20 MHz harmonics down at least 70 db (less than - 40 dbm).
If a Auto Het operation malfunction indicates that the 200 MHz Power Amplifier is out of alignment or a component has been replaced that effects its operation, perform the alignment procedure in Table 4-8. Figure 4-6 illustrates the adjustment holes drill out location and the adjustment callouts. Figure 4-7 illustrates a Spectrum Analyzer display of the Power Amplifiers output on a Tektronix 7L12 Plug-in Spectrum Analyzer in a 7000 series Oscilloscope main frame.

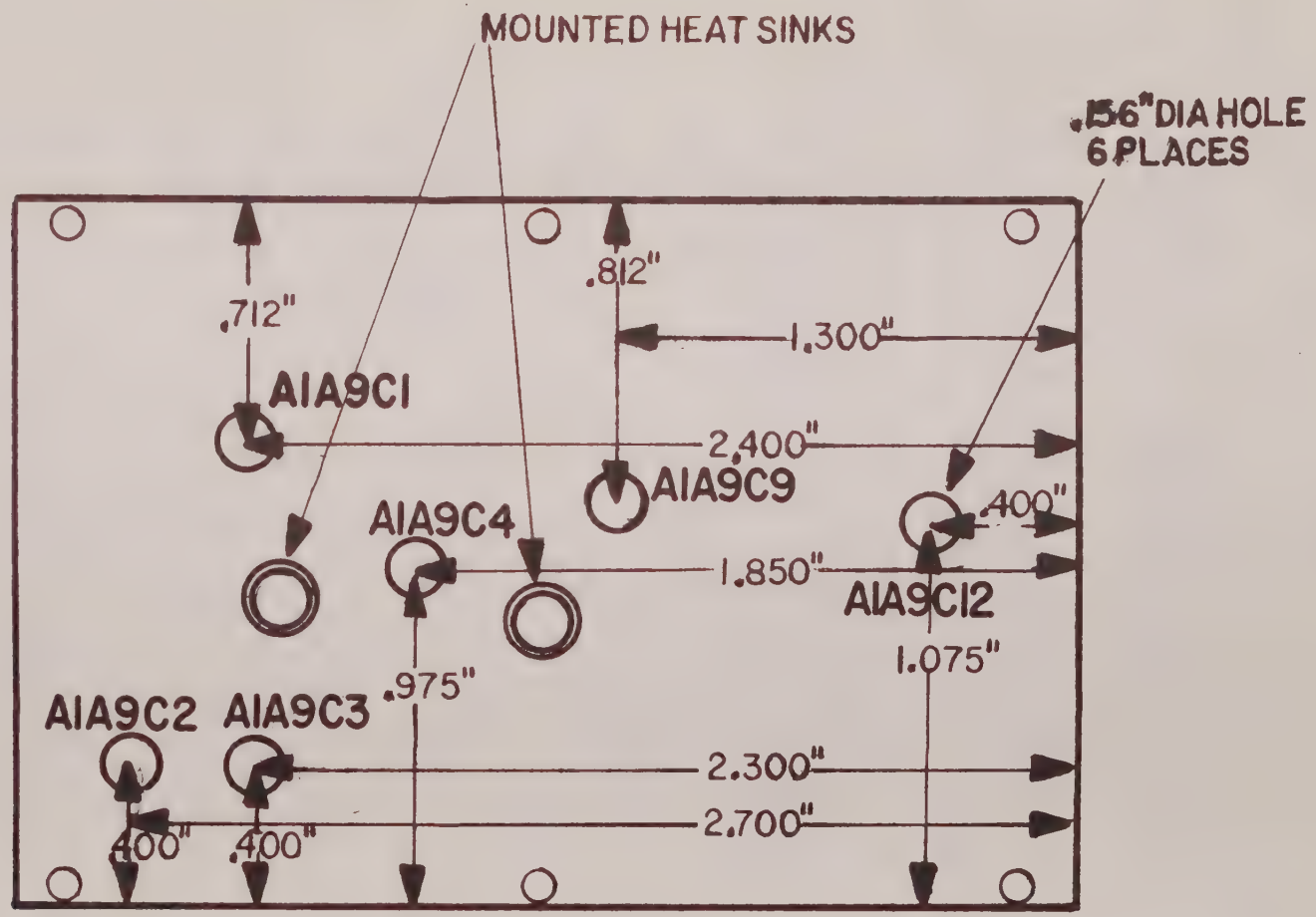


FIGURE 4-6
200 MHZ POWER AMPLIFIER ASSEMBLY COVER PLATE WITH
ADJUSTMENT ACCESS HOLES DRILLING LOCATION
AND ADJUSTMENT CALLOUTS

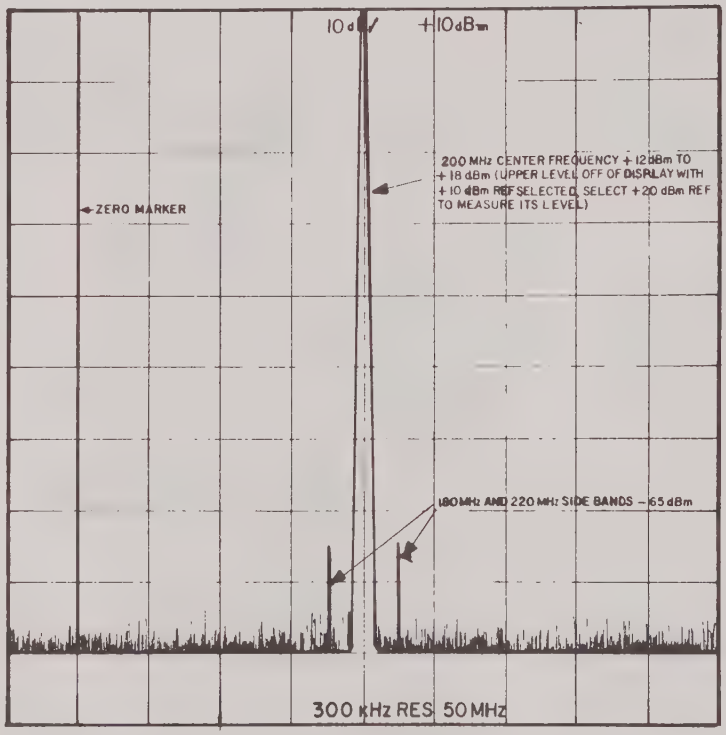

10 dB/
+10dBm
200 MHz CENTER FREQUENCY + 12 dBm TO
+ 18 dBm (UPPER LEVEL OFF OF DISPLAY WITH
+ 10 dBm REF SELECTED, SELECT +20 dBm REF
TO MEASURE ITS LEVEL)
ZERO MARKER
180 MHz AND 220 MHz SIDE BANDS – 65 dBm
300 kHz RES 50 MHz

FIGURE 4-7
200 MHZ POWER AMPLIFIER OUTPUT SPRECTRUM

TABLE 4-8

200 MHZ POWER AMPLIFIER ADJUSTMENT PROCEDURE

STEP	ACTION
1	Verify that the 200 MHz Frequency Multiplier A1A11 is outputing the proper signal with a Spectrum Analyzer, (TEK 7L12 w/ 7000 series main frame or equivelent) at A1A11 output connector. Refer to Table 4-7 step 2 and Figure 4-5B for the signal requirements.
2	Monitor the output of the 200 MHz Power Amplifier at its SMA output coax connector with a Spectrum Analyzer to verify that its output signal is actually out of the required parameters. The signal must be 200 MHz at a level of 1.5 Watts (+31 dBm) or greater and the side bands must be 70 dB down (less than -40 dBm), refer to Figure 4-7 for the proper Spectrum display. Do not attempt to adjust the 200 MHz Power Amplifier for improved side band rejection or increased output if it is within the proper parameters. On the other hand if the above parameters are not met perform the adjustments by proceeding to step 3.
3	From the bottom of the Auto Het chassis A1, remove the two 4-40 mounting screws that secure the 200 MHz Power Amplifier to the chassis.
4	From the top of the instrument lift the A1A9 assembly upward and rotate it clockwise 90^0 in the horizontal plane, and then place it on top of the A1 chassis.
5	Remove the side cover plate from the A1A9 assembly and drill six .156" (5/32") holes to provide adjustment access to the PCB mounted trimmer capacitors. Refer to Figure 4-6 for the drilling center location dimensions.
6	Dress the drilled holes to remove any burrs, and replace the cover plate on the assembly making sure that the heat sinks align and slip on to transistors A1A9Q1 and Q2. Replace the six 2-56 and secure the cover plate to the assembly.
7	Refer to Figure 6-13 the 200 MHz Power Amplifier Schematic Diagram making note of the following listed trimmer capacitors and their circuit relationships.

TABLE 4-8

200 MHZ POWER AMPLIFIER ADJUSTMENT PROCEDURE

Continued

STEP	ACTION
	1. A1A9C12 Input coupling circuit adjustment; provides the adjustment of A1A9Q1 tuned base circuit. 2. A1A9C9; A1A9Q3 collector tuned circuit tuning capacitor. 3. A1A9C4; A1A9Q2 collector tuned circuit tuning capacitor. 4. A1A9C3; A1A9Q1 input base coupling circuit trimmer capacitor. 5. A1A9C1; A1A9Q1 collector tuned circuit trimmer capacitor. 6. A1A9C2; Output coupling circuit tuning capacitor. From the above descriptions of the trimmer capacitor's circuit relationship it should be noted that intereaction of the adjustments will require a see-saw technique trimming for proper effect and not a inline step procedure to adjust the circuits.
8	With a non-metallic alignment tool alternately adjust the trimmer capacitors for the required output parameters, by monitoring the output signal on a Spectrum Analyzer.
9	When a output signal that meets or exceeds the parameters is obtained, remove the assembly cover plate, and seal the adjustment access holes that were drilled, by taping and screwing in plugs, or inserting snap button hole (Butch) plugs.
10	Replace the assembly's cover plate, remount the A1A9 assembly to the Auto Het chassis and reconnect the coax cable to the assembly's output connector.

4.3.9 D/A Convertor and YIG Driver/ Controller Alignment.

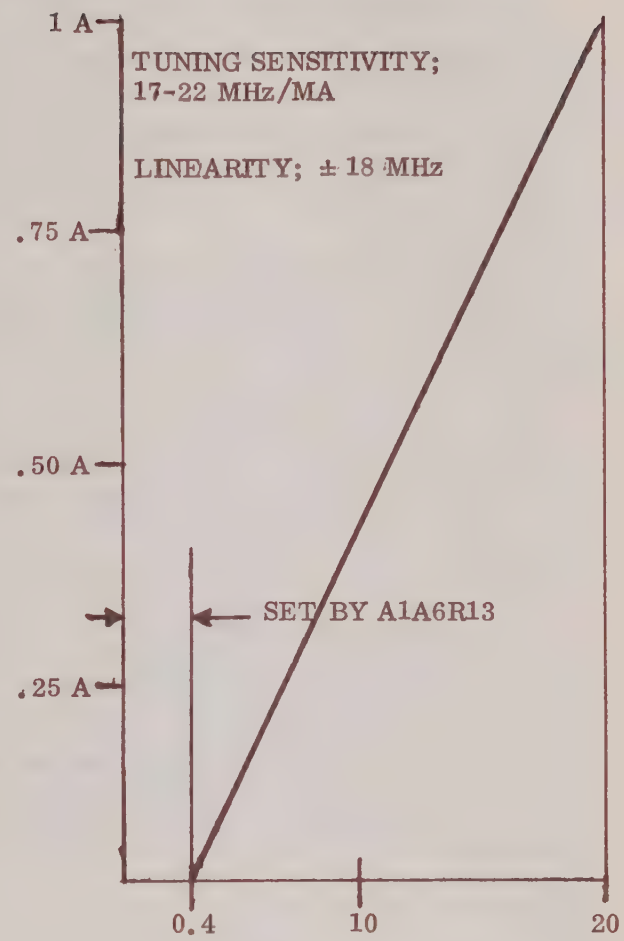
The alignment of the YIG ramp and the YIG drive control signals are provided for by three potentiometer adjustments that interreact and thus will mutally effect the YIG Tuned Multipliers assembly output signal. These controls are factory set to obtain a 200 MHz comb line YIG output generation of .4-to-13.4 GHz for the Model 988A and .4-to18.0 GHz for the Model 989A counter, with a proper output leveling. Refer to Table 3-4 page 3-10 and Figure 3-2 page 3-11 for the YIG Tuned Multioctave Multiplier output specifications.

The D/A Convertor and YIG Driver/ Controller alignment should be made only if the YIG Tuned Multiplier assembly (A8) is replaced. Or if a component has been replaced in the 200 MHz Power Amplifier (A1A9), the YIG Driver and Controller (A1A6) or the D/A Converter (A1A5) that effects operation of the YIG.

The aligment controls are listed below with a description of there functions and circuit relationships to aid the technician in there proper adjustments.

RAMP CALIBRATION control (A1A5R42); a 1KΩ potentiometer that sets the gain of the D/A Convertors Summation Amplifier (A1A5U5) and determines the amplitude of the D/A Convertors output ramp.

LOW FREQUENCY ADJUSTMENT (A1A6R13); a 1KΩ potentiometer that sets the offset of the I.C. Operational Amplifier (A1A6U1), and will determine the low frequency limit (first comb line) of the YIG Tuned Multiplier. The illustration below provides a graph of the YIG output frequency verses the YIG tuning current and indicates the effect of the LOW FREQUENCY ADJUSTMENT on the current ramp.



YIG POWER LEVELING ADJUSTMENT (A1R2) a 50Ω potentiometer mounted on the Auto Het RF chassis near the YIG assembly. This control will set the level of the voltage ramp which is applied as V_{cc} to the last two amplifier stages of the 200 MHz Power Amplifier assembly (A1A9). This in effect sets the output level of the 200 MHz drive signal to the YIG.

The following procedure is provided to allow for the proper adjustment of the YIG Tuned Multiplier output.

1. Remove the coax cable from connector A1A7J1 to disable the generation of the STOP command.
2. Connect a Spectrum Analyzer having a .4-to-18 GHz range to the YIG Tuned Multipliers output connector.
3. Input a valid Range 3 test signal from a signal generator that will provide midscale deflection on the INPUT LEVEL meter, this will generate a START command and allow the Sweep Generator (A1A3) to free run.
4. Note the frequency of the first comb line on the Spectrum Analyzer display, it should be 0.4 GHz adjust the LOW FREQUENCY control (A1A6R13) to obtain a .4 GHz YIG lower limit output.
5. Insure that the YIG is outputing 200 MHz comb lines from the lower limit set (.4 GHz) to 13.4 GHz (18GHz on the Model 989A) if not, adjust the RAMP CALIBRATION control (A1A5R42) for a proper YIG output. Interraction between A1A5R42 and A1A6R13 may be incountered and will require repeating steps 4 and 5 a number of times to obtain the proper YIG comb output.
6. On the Spectrum Analyzer display, note the power level of the complete comb spectrum, the power level should be within -3 dBm at .4GHz to < - 32 dBm at 13.4 GHz (18GHz for the Model 989A). And the power output of adjacent comb lines should not vary by more than 5 dB. If the power output level does not meet the above parameters, adjust the POWER LEVELING control (A1R2) for the proper power output.
7. Disconnect the test configuration and reconnect the coax cable to connector A1A7J1 and verify the operation of the counter in Range 3 by inputing a valid test signal at different frequencies from .6 GHz to 13.4 GHz.

4.4 TROUBLESHOOTING AND REPAIR TECHNIQUES

This subsection provides the basic information to determine the nature and location of an instrument fault or failure, and provides the repair techniques for removing and replacing component parts of the counter.

4.4.1 Troubleshooting

Troubleshooting the Microwave Counter is accomplished at three levels. The first level is to sectionalize the failure to a subassembly or functional area of the counter. Once isolated to a particular subassembly or functional area, the second level or localization of the problem is undertaken to confine the fault to an individual circuit function or a plug in PCB board. The third level or isolation involves the actual location of a defective component part within a functional stage or individual circuit.

In the event of a suspected failure and before any troubleshooting or repairs are attempted:

1. Insure that the applied input signal that is being measured is of sufficient amplitude and within the specified range (refer to the input characteristics of the specification in Section 1 of this manual, located on pages 1-5 and 1-6).

2. Verify that the operating controls are properly positioned for the measurement being attempted.

If the problem is not operator error and a valid malfunction is encountered, then examine the counter for the following observable characteristics:

1. Does the Counter fail to turn-on:

   a. No display
   b. No fan operation
   c. No GATE lamp illumination

2. Does the Counter fail to operate in all ranges or is the malfunction limited to only one range.

4.4.2 Malfunction at Turn-On.

If the counter fails to turn-on, make the following checks:

1. POWER switch is set to ON?

2. Power cord is plugged into the counter and an appropriate power source?

3. Does the ac power source have the correct voltage and line frequency for proper instrument operation?

4. Is the rear panel line fuse A5F1 good?

5. Is the input line filter/connector assembly A5FL1/J4 good?

6. Check ac power distribution wiring and its load components listed below:

   a. POWER ON/OFF switch A4S1
   b. Power Transformer A5T1
   c. Fan motor A5B1
   d. 1 MHz Reference Oscillator internal heater element.

If overheating or wiring fault is indicated, repair or replace as required.

4.4.3 IC Troubleshooting Techniques.

When troubleshooting circuits built from discrete components, the task is one of verifying relatively simple characteristics such as resistance, capacitance, or turn-on voltages of components with two or at most three nodes. While the function of the total circuit may be quite complex, each component in that circuit performs a relatively simple task and proper operation is easily verified. In Figure 4-8, each diode, resistor, capacitor, and transistor can be tested using a signal generator and a voltmeter, ohmmeter, diode checker, or oscilloscope--the traditional troubleshooting tools. But when this circuit is built in integrated circuit form, these components are no longer accessible. It now becomes necessary to test the operation of the complete circuit function.

Thus, the important difference between discrete circuitry and circuits developed from digital IC's is in the complexity of the functions performed by the IC's. Unlike the resistor, capacitor, diode or transistor, which must be interconnected to form a circuit function, the

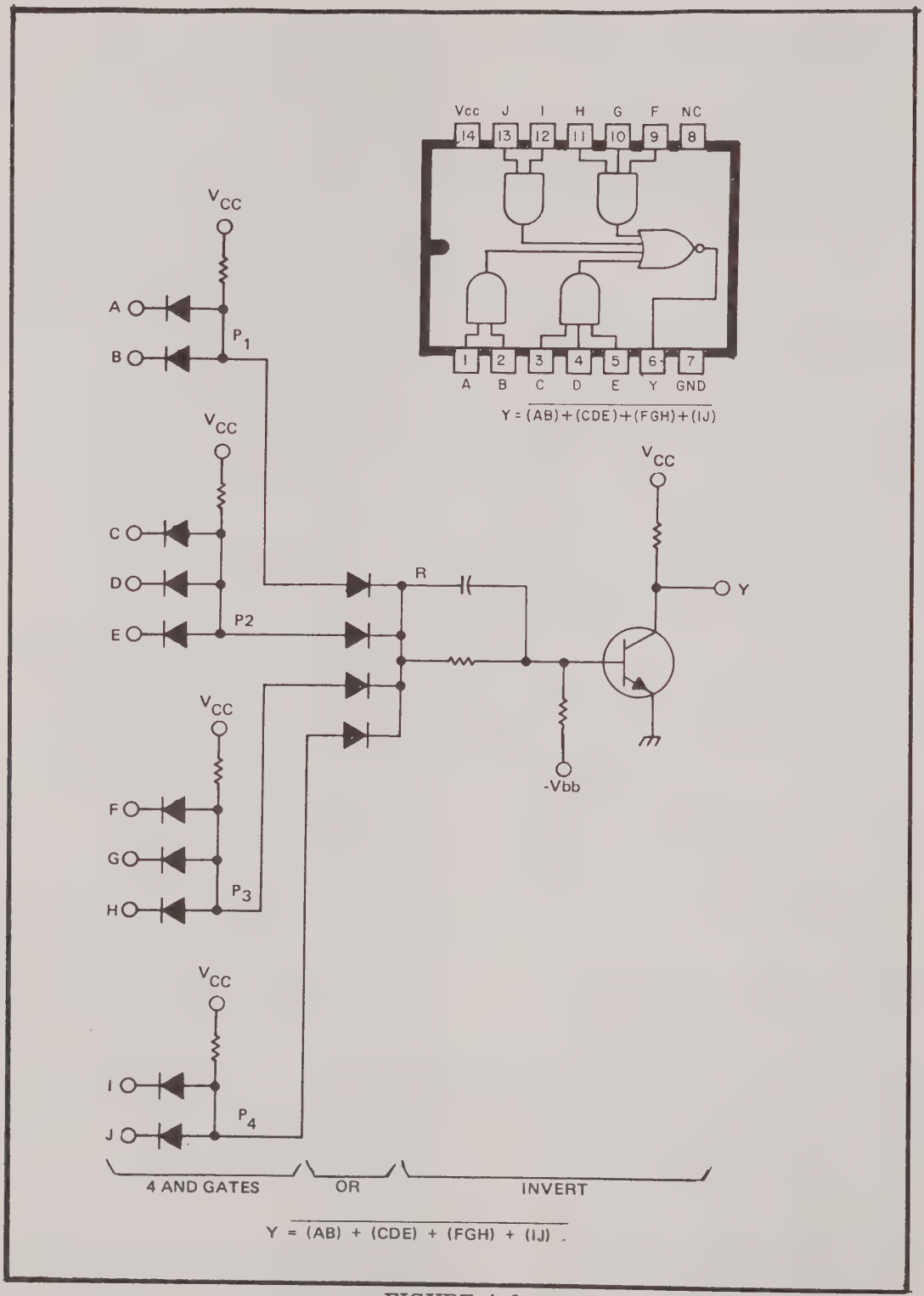


FIGURE 4-8
DISCRETE VS INTEGRATED CIRCUITS

digital IC performs complete complex functions. Instead of observing simple characteristics, it becomes necessary to observe complex digital signals and then decide if these signals are correct and will provide the function that the IC was designed to perform.

Verifying proper IC operation requires stimulating and observing many inputs (in Figure 4-8 there are 10 inputs) while simultaneously observing several outputs (often 2 or 3 and at times as many as 10). Thus, the fundamental difference between circuitry built from discrete components and digital IC's is the number of inputs and outputs associated with each component and the need to stimulate and observe these simultaneously.

In addition to the problems of simultaneity of signals and complexity of functions at the component level, the digital IC has introduced a new degree of complexity at the circuit level. Circuits which perplex all but their designer are commonplace. Given enough time, these circuits can be studied and their operation understood, but this is not an affordable luxury for those involved in troubleshooting electronic circuits. Without understanding a circuit's intricate operation it becomes necessary to have a technique of quickly testing each IC element rather than attempting to isolate a failure to a particular circuit segment by testing for expected signals.

Troubleshooting circuits configured from discrete components requires verifying characteristics such as resistance, capacitance, or transistor turn-on voltages. To troubleshoot a digital IC the output(s) are verified to the inputs as defined by the Boolean equation of the IC logic functions, or by the use of a truth table.

In order to solve these problems and to make the troubleshooting of digital circuits more efficient, it is necessary to take advantage of the digital nature of the signals involved. To aid the technican in troubleshooting IC functions the following IC data sheets are provided on each type of IC used in the Model 988/989 Microwave Counter.

TABLE 4-9

INTEGRATED CIRCUIT DATA SHEETS

CIRCUIT TYPE	FUNCTION	FIG. NO.
SN7400	Quad 2-Input Positive NAND Gates	4-9
SN7402	Quad 2-Input Positive NOR Gates	4-10
SN7403	Quad 2-Input Positive NAND Gates (with open-collector output)	4-11
SN7404	Hex Inverters	4-12
SN7405	Hex Inverters (with open collector output)	4-13
MC836F, P	Hex Inverters	4-14

Table 4-9 Integrated Circuit Data Sheets (Continued)

MC3008L, P	Hex Inverters	4-15
SN7410	Triple 3-Input Positive NAND Gates	4-16
SN7440	Dual 4-Input Positive NAND Gates/Buffers	4-17
SN7442	4-Line-to-10 Line Decoder (1-of-10)	4-18
SN7451	Expandable Dual 2-Wide, 2-Input AND-OR-Invert Gates	4-19
SN7454	Expandable 4-Wide, 2-Input AND-OR-Invert Gates	4-20
SN7473/74107	Dual J-K Master-Slave Flip-flops	4-21
SN7475/5475	4-Bit Bistable Latches	4-22
SN7486/54L86	Quad 2-Input Exclusive-OR Gates	4-23
SN7490	Decade Counter	4-24
SN7493	4-Bit Binary Counter	4-25
SN74121	Monostable Multivibrator	4-26
SN74141	BCD-to-Decimal Decoder/Driver	4-27
SN74196	50 MHz Presettable Decade and Binary Counter/Latch	4-28
MC846F, P	Quad 2-Input NAND Gates	4-29
MC1039	ECL to TTL Quad Translators	4-30
MC1663	ECL Quad 2-Input NOR Gates	4-31
MC1661	ECL Dual 4-Input Gate	4-32
MC3062F/ 3062L, P	Dual J-K Flip-flop	4-33
MC4044, L, P	Phase-Frequency Detector	4-34
MC10131/10231	ECL Dual Type D Master-Slave Flip-flop	4-35

Table 4-9 Integrated Circuit Data Sheets (Continued)

CA 3049	Dual Independent Differential RF/IF Amplifier	4-36
LM109, 209, 309(K)	5 Volt Monolithic Voltage Regulator	4-37
LM301AN, SN52101A, SN72301A	High-Performance Operational Amplifiers	4-38
LM307, SN52107, SN72307	High-Performance Operational Amplifiers	4-39
LM471, SN52741	High-Performance Operational Amplifiers	4-40

The following IC Data Sheets provides two or more of the following listed informational items on each type(s) of IC used in the Model 988/989 Microwave Counter.

1. Device outline and pinning data.

2. A Logic diagram of the IC device. On the less complex devices, the logic diagram is included within the device outline/pinning diagram.

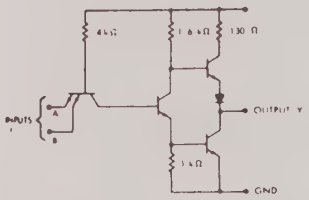
3. A Boolean equation of the device function(s).

4. Truth Tables providing input/output digital state relationships.

5. Schematic equivalents in discrete component form of the device. In most cases the schematic equivalent shows only one element of the IC, if the other elements are the same.

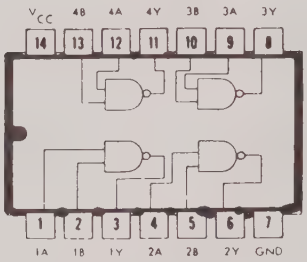
CIRCUIT TYPE SN7400
QUADRUPLE 2-INPUT POSITIVE NAND GATES

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

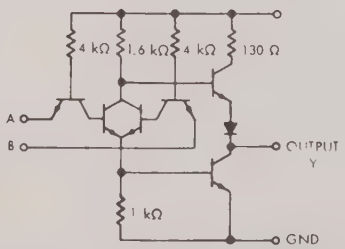


positive logic: $Y = \overline{AB}$

FIGURE 4-9

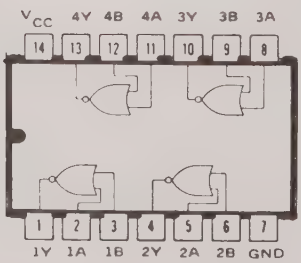
CIRCUIT TYPE SN7402
QUADRUPLE 2-INPUT POSITIVE NOR GATES

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)

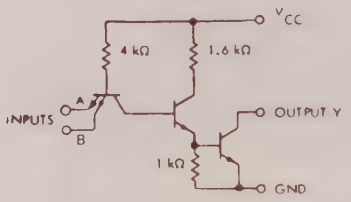


positive logic: $Y = \overline{A + B}$

FIGURE 4-10

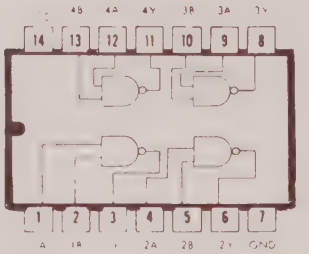
CIRCUIT TYPE SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

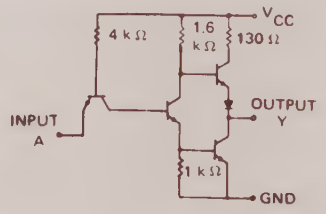


positive logic: $Y = \overline{AB}$

FIGURE 4-11

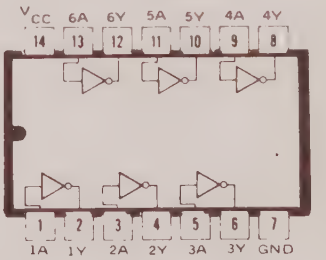
CIRCUIT TYPE SN7404
HEX INVERTERS

schematic (each inverter)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

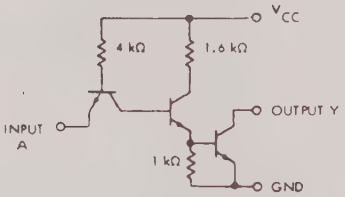


positive logic: $Y = \overline{A}$

FIGURE 4-12

CIRCUIT TYPE SN7405
HEX INVERTERS (WITH OPEN-COLLECTOR OUTPUT)

schematic (each inverter)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

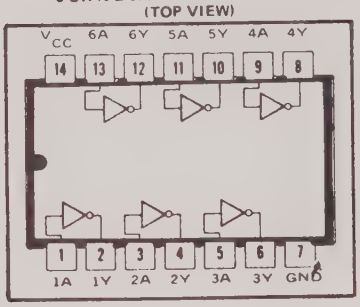
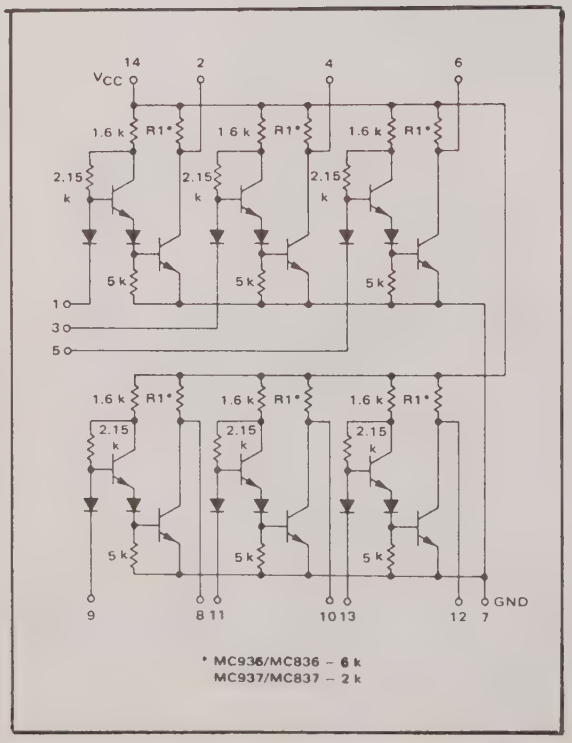


FIGURE 4-13

CIRCUIT TYPE MC836F, P
HEX INVERTERS



This element consists of six inverter circuits.

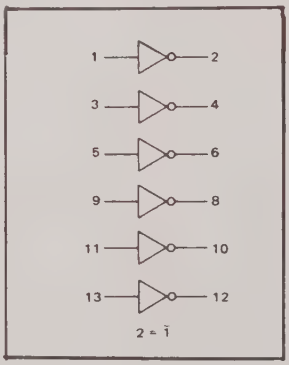


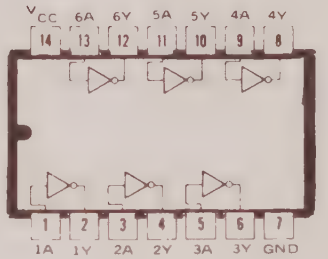
FIGURE 4-14

CIRCUIT TYPE MC3008L,P

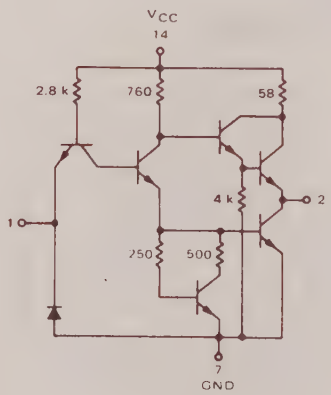
HEX INVERTERS

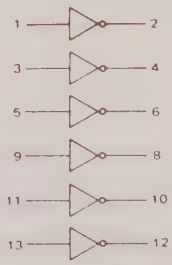
This device offers six independent inverting gates in a single package. Each gate consists of a single input driving an output inverter.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



1/6 OF CIRCUIT SHOWN





Positive Logic: $2 = \overline{1}$

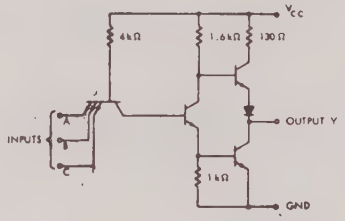
Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 140 typ/pkg
Propagation Delay Time = 6 ns typ

FIGURE 4-15

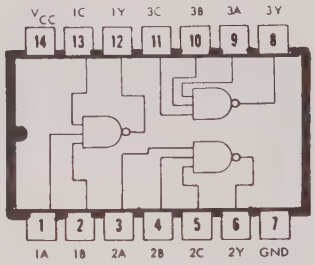
CIRCUIT TYPE SN7410
TRIPLE 3-INPUT POSITIVE NAND GATES

schematic (each gate)



NOTE: Component values shown are nominal

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

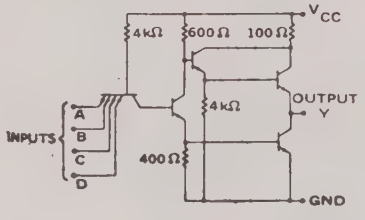


positive logic: $Y = \overline{ABC}$

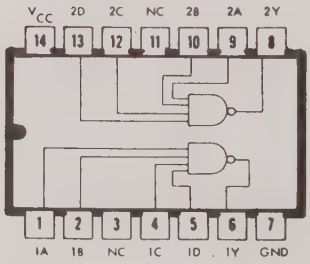
FIGURE 4-16

CIRCUIT TYPE SN7440
DUAL 4-INPUT POSITIVE NAND BUFFERS

schematic (each gate)



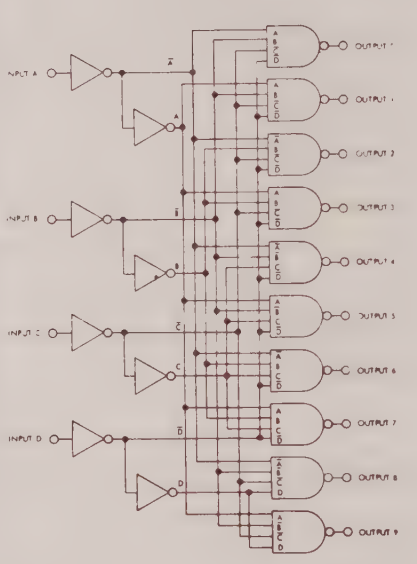
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



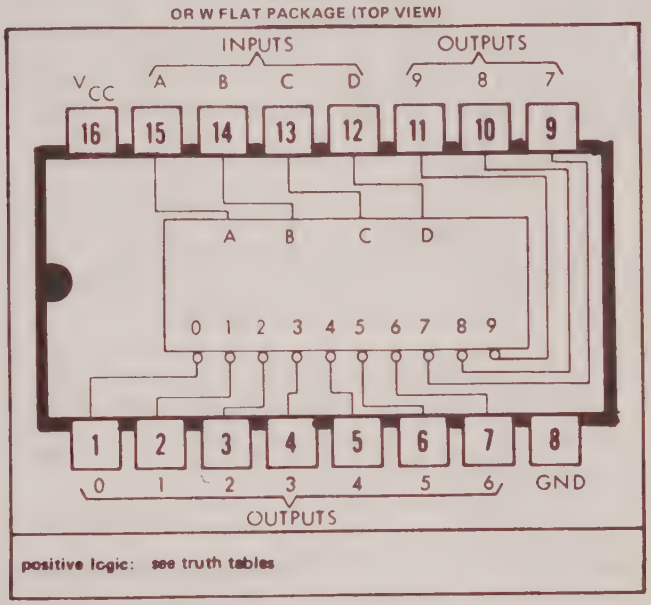
positive logic: $Y = \overline{ABCD}$

FIGURE 4-17

CIRCUIT TYPE SN7442
4-LINE-TO-10-LINE DECODERS (1-OF-10)



J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



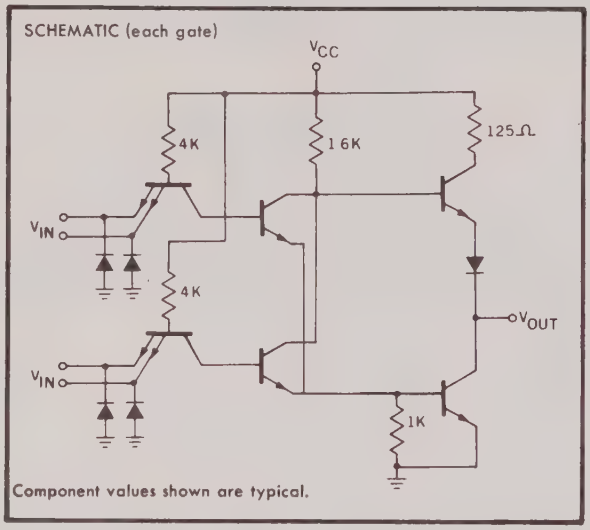
positive logic: see truth tables

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

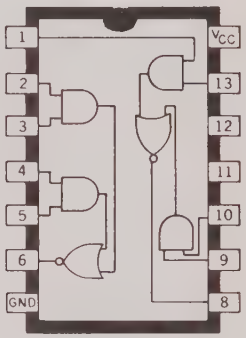
BCD INPUT				DECIMAL OUTPUT									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

FIGURE 4-18

CIRCUIT TYPE SN7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



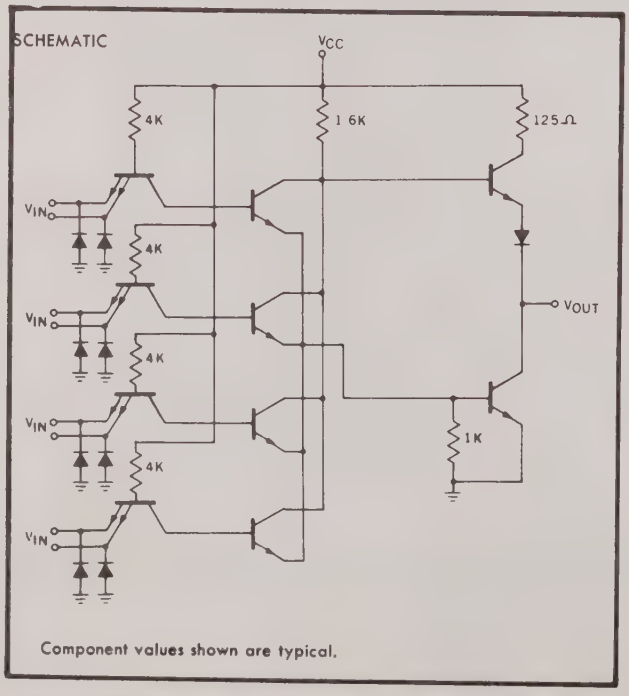
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



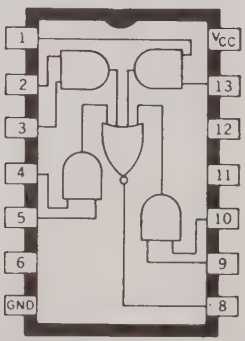
positive logic: $Y = \overline{(AB) + (CD) + (X)}$

FIGURE 4-19

CIRCUIT TYPE SN7454
EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATES



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



$Y = \overline{(AB) + (CD) + (EF) + (GH) + (X)}$

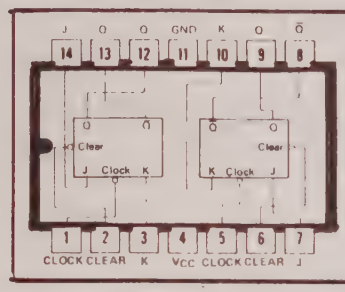
FIGURE 4-20

CIRCUIT TYPES SN7473, SN74107
DUAL J-K MASTER-SLAVE FLIP-FLOPS

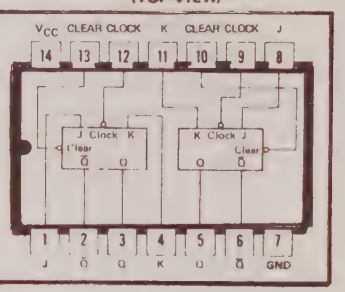
TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse

SN5473, SN7473
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



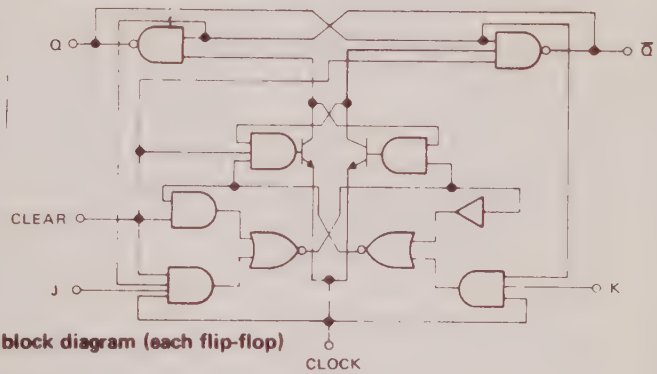
SN54107, SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
Low input to clear sets Q to logical 0.
Clear is independent of clock.

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



functional block diagram (each flip-flop)

schematic (each flip-flop)

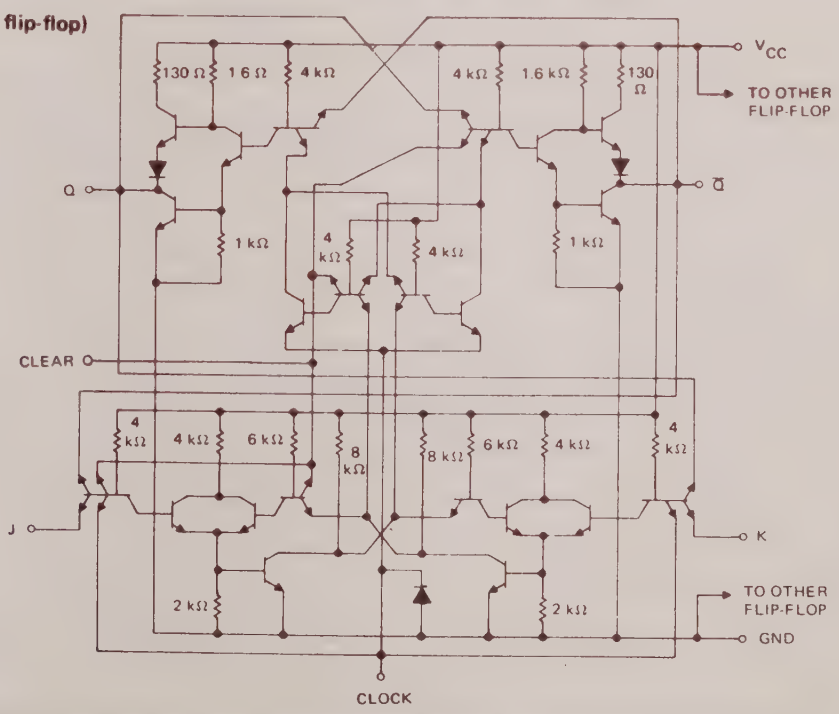
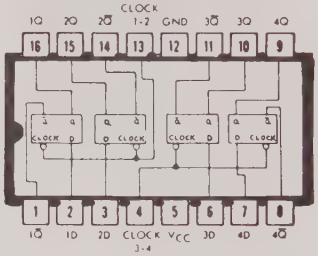


FIGURE 4-21

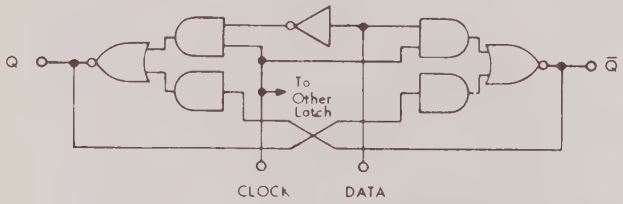
CIRCUIT TYPE SN5475
4-BIT BISTABLE LATCHES

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

SN5475/SN7475
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



functional block diagram (each latch)

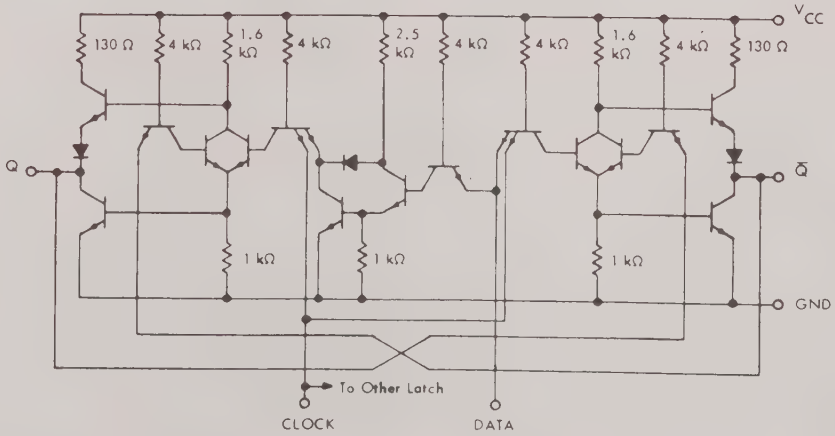


TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative going transition.

NC—No internal connection

schematic (each latch)



Component values shown are nominal.

FIGURE 4-22

CIRCUIT TYPE SN54L86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

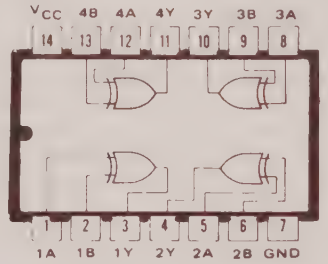
positive logic: $Y = A \oplus B$

$Y = A\bar{B} + \bar{A}B.$

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW



Each of these low-power, monolithic, quadruple 2-input exclusive–OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary the output goes to a logical 1.

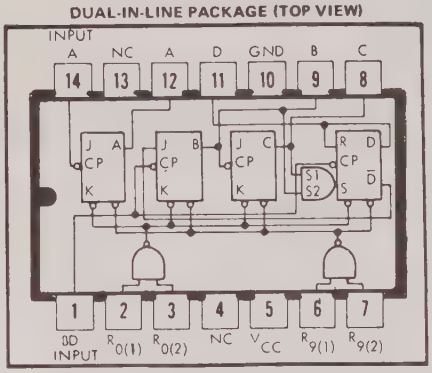
These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

FIGURE 4-23

CIRCUIT TYPE SN7490

DECADE COUNTERS

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

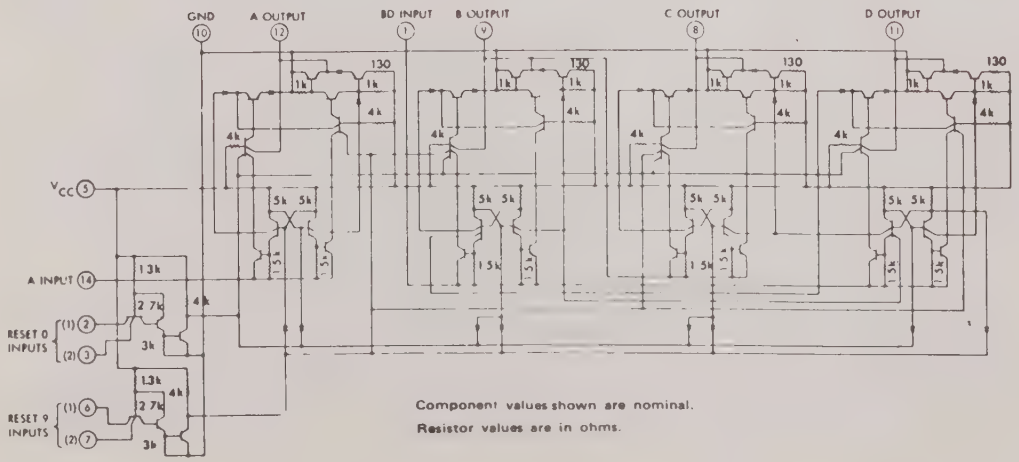
These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

schematic



Component values shown are nominal.
Resistor values are in ohms.

FIGURE 4-24

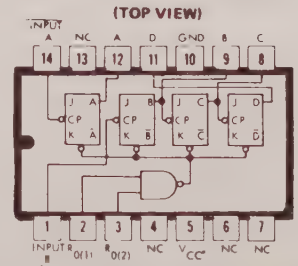
CIRCUIT TYPE SN7493
4-BIT BINARY COUNTERS

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES:
1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

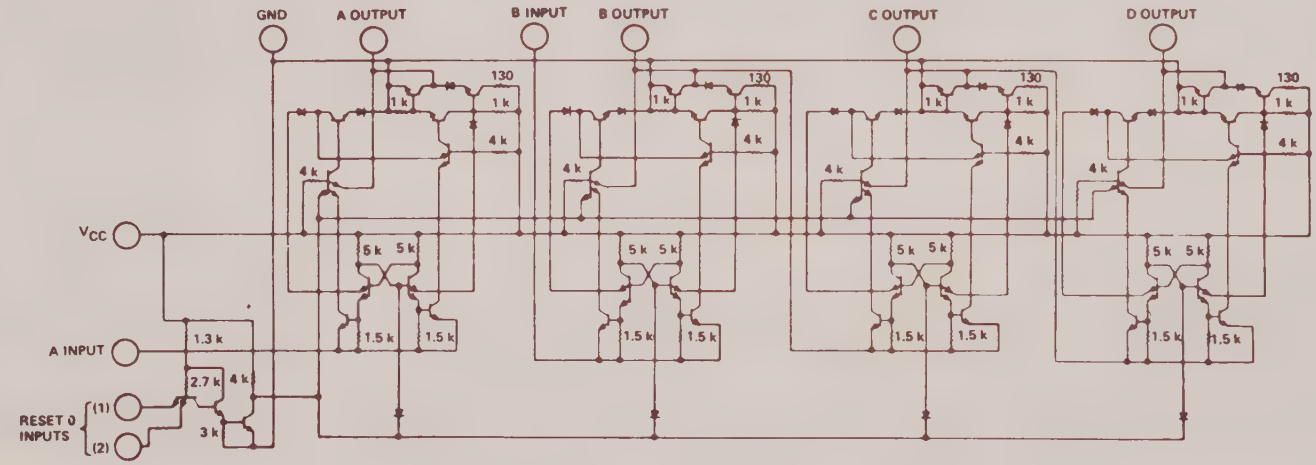


FIGURE-4-25

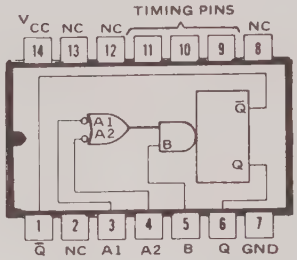
CIRCUIT TYPE SN74121
MONOSTABLE MULTIVIBRATORS

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$

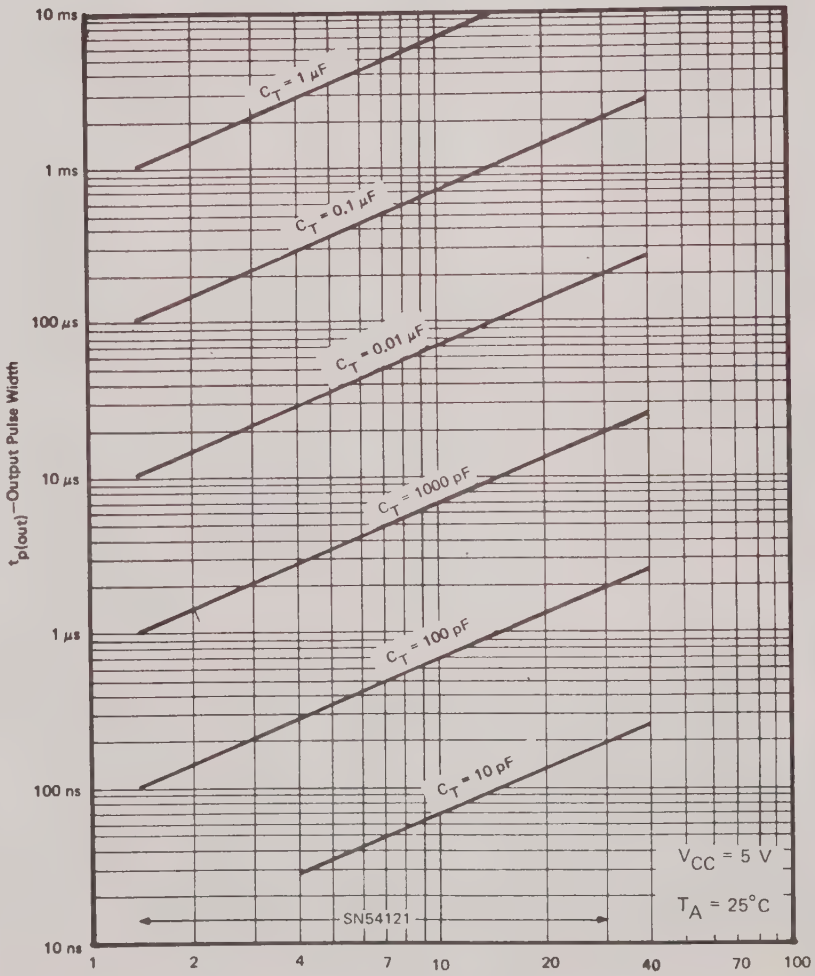
$0 = V_{in(0)} \leq 0.8\ V$

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NOTES:

1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a logical 0 or 1 may be present.
4. NC = No Internal Connection.
5. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).
9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.

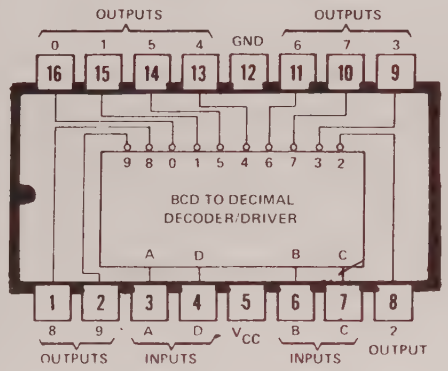


OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

FIGURE 4-26

CIRCUIT TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
†All other outputs are off

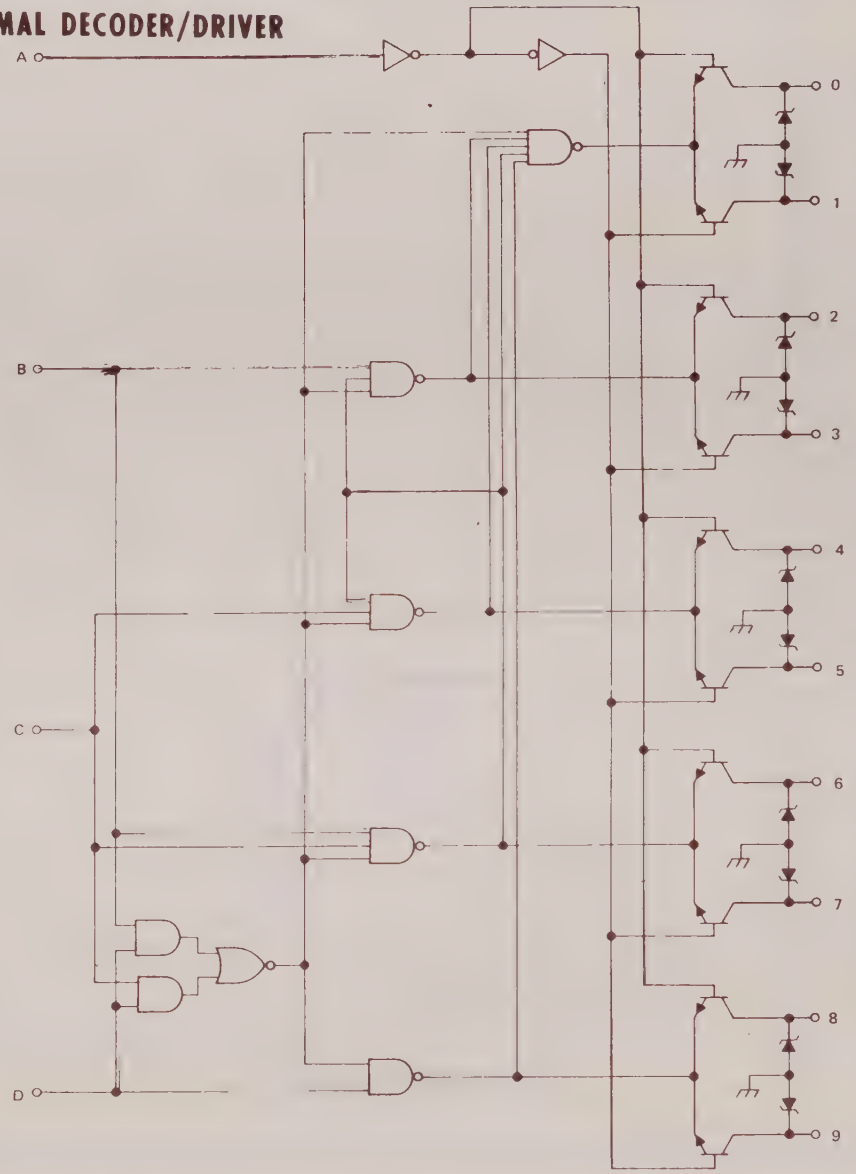
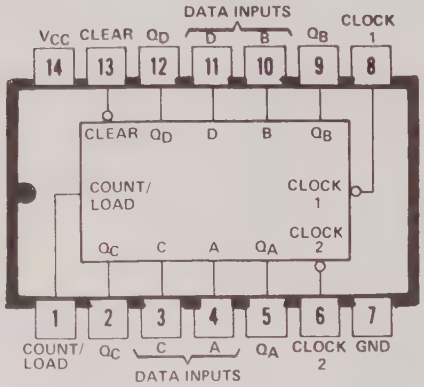
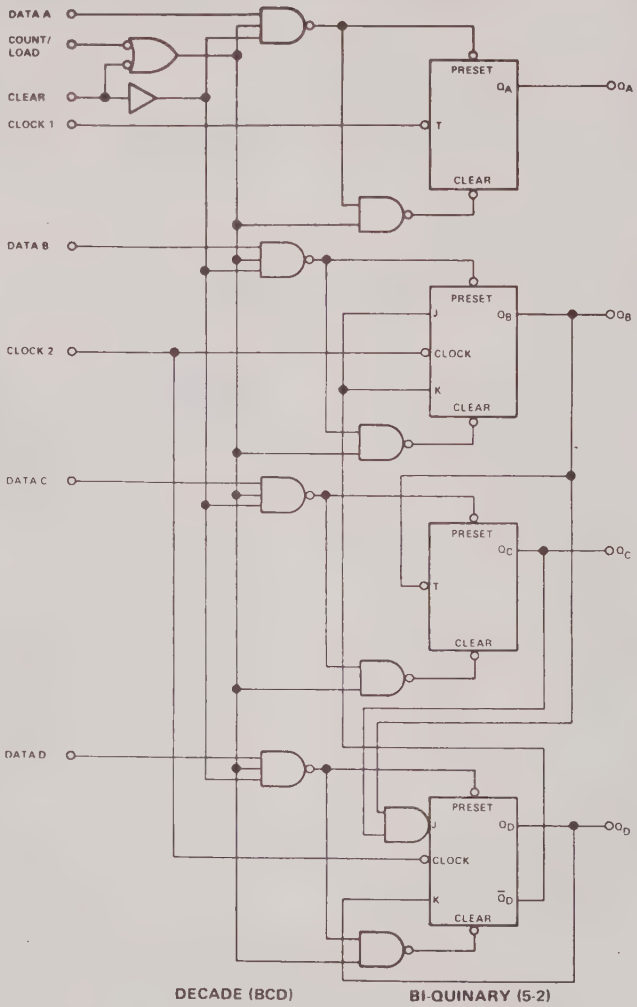


FIGURE 4-27

CIRCUIT TYPE SN74196
50-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)


DATA INPUTS
VCC CLEAR QD D B QB CLOCK 1
14 13 12 11 10 9 8
CLEAR QD D B QB
COUNT/ LOAD
CLOCK 1
CLOCK 2
QC C A QA
1 2 3 4 5 6 7
COUNT/ LOAD QC C A QA CLOCK 2 GND
DATA INPUTS



The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.

DECADE (BCD) (See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

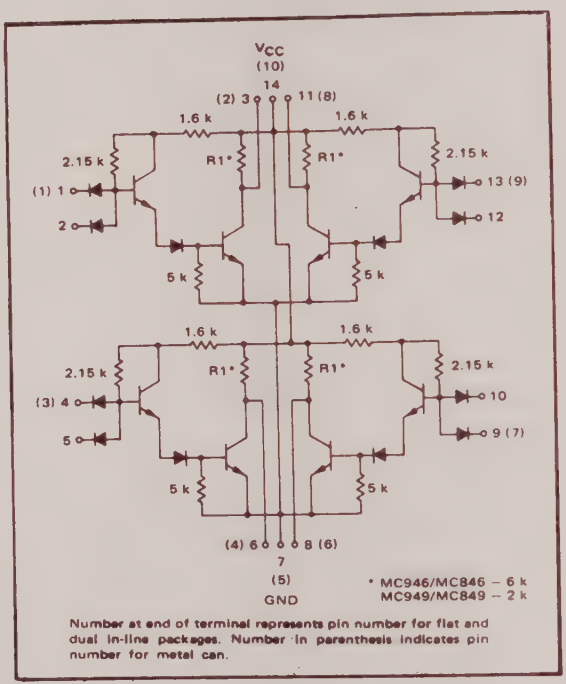
NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

FIGURE 28

CIRCUIT TYPE MC846F, P

QUAD 2-INPUT "NAND" POWER GATE



This gate element, in the 14-pin flat and dual in-line packages, consists of four 2-input NAND gate circuits. This circuit can be used as a dual 2-input non-inverting gate, or as two bistable circuits when two dual 2-input gates are cross-coupled.

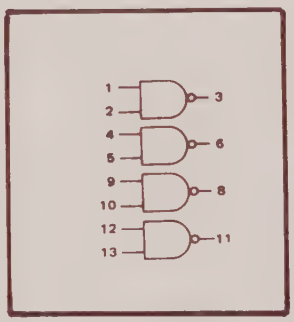
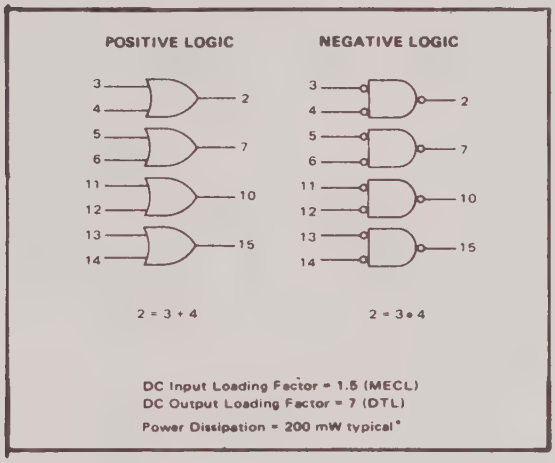


FIGURE 29

CIRCUIT TYPE MC1039

**MECL-TO-SATURATED LOGIC
QUAD TRANSLATORS**

Level translator for converting MECL signal levels to saturated logic levels. The four independent translators provide the positive logic OR function. The devices are available in the 16-pin packages.



DC Input Loading Factor = 1.5 (MECL)
DC Output Loading Factor = 7 (DTL)
Power Dissipation = 200 mW typical*

CIRCUIT SCHEMATIC

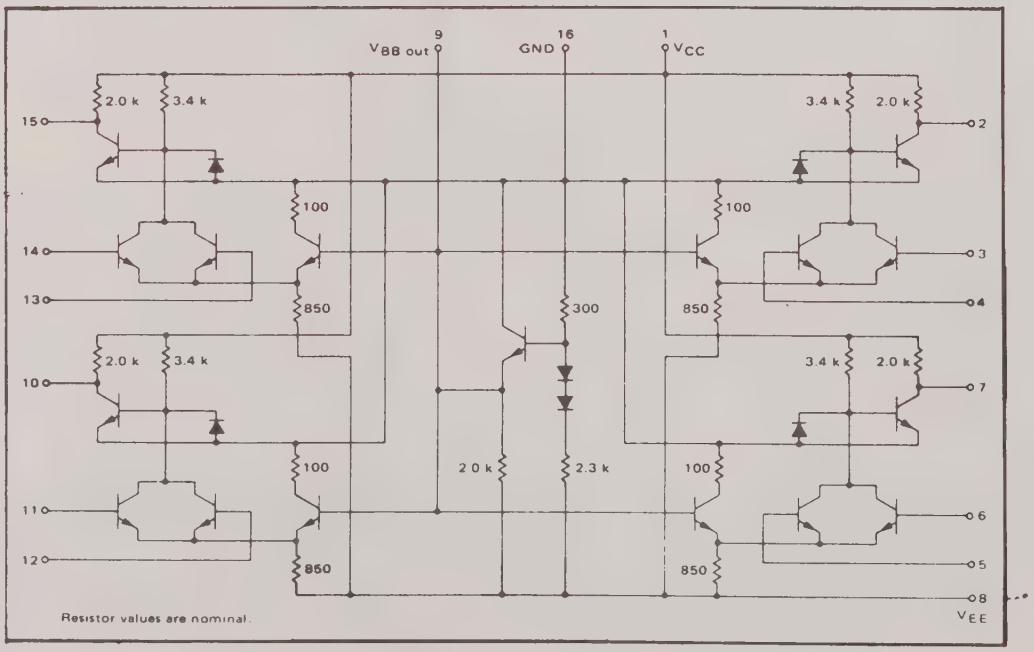


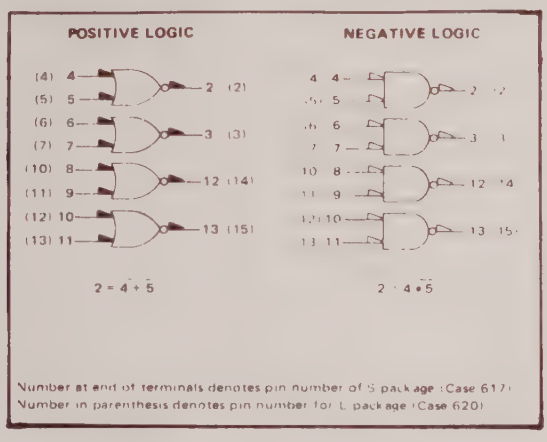
FIGURE 30

CIRCUIT TYPE MC1663

QUAD 2-INPUT "NOR" GATE

This device consists of four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (0 to +75°C).

Input pulldown resistors of 2.0-k ohms eliminate the need to tie unused inputs to V_{EE} and act as a local load for other MECL III devices. The "Low-Z" device designation is attributed to the 2.0-k ohm value of the input pulldown resistors.



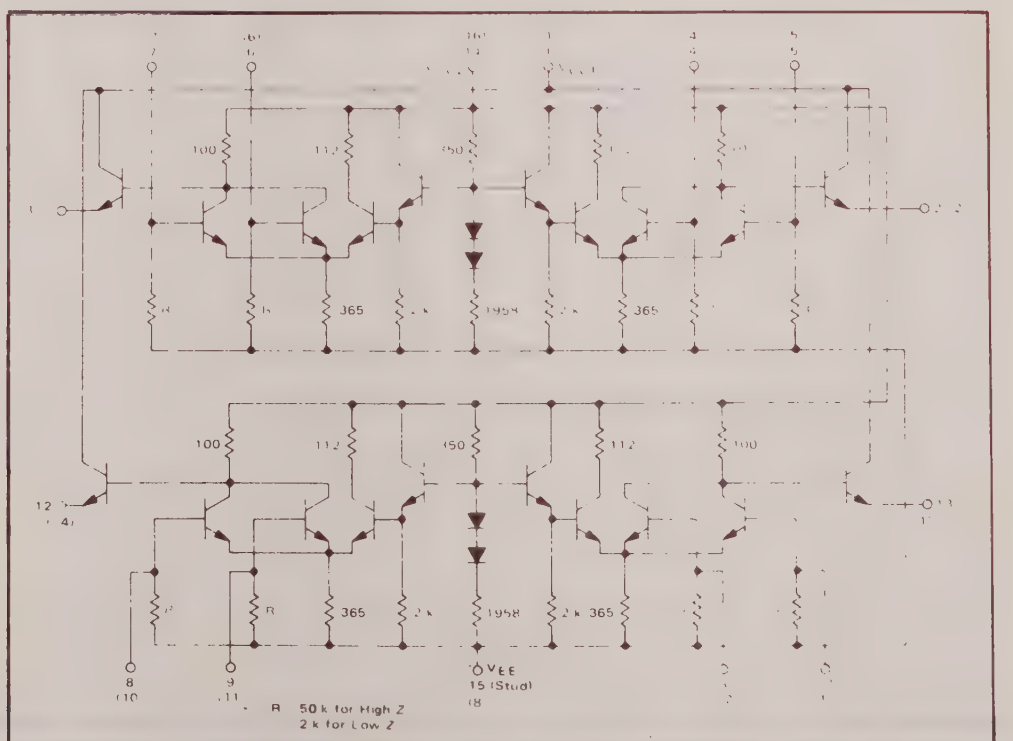


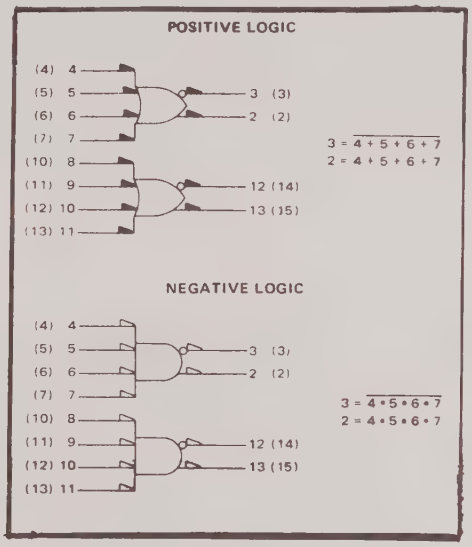
FIGURE 31

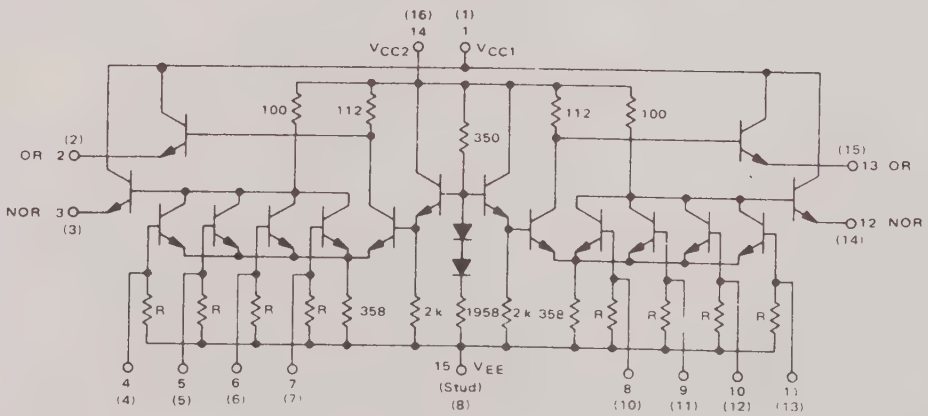
CIRCUIT TYPE MC1661

DUAL 4-INPUT GATE (LOW Z)

This device provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point remains in the center of the transition region over the temperature range (0 to +75°C).

Inclusion of the 2.0-k ohm input pulldown resistors eliminates the need to tie unused inputs to V_{EE}, and they may also be utilized to act as a local load for another MECL III device. The "Low Z" device designation is attributed to the 2.0-k ohm value of these input pull-down resistors.





Numbers at ends of terminals denote pin numbers for S package (Case 617)
Numbers in parenthesis denote pin numbers for L package (Case 620)

R = 50 k (High Z)
2 k (Low Z)

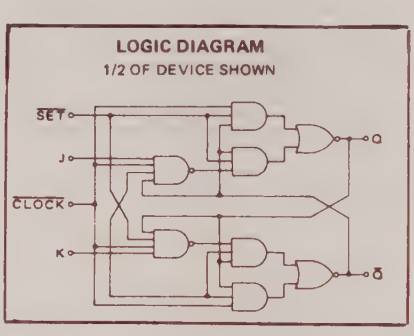
FIGURE 32

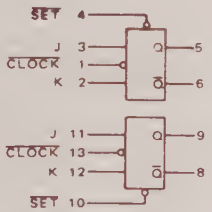
CIRCUIT TYPE MC3062F MC3062L,P

DUAL J-K FLIP-FLOP

This dual JK flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a seperate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip-flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the $\overline{SET}$ input.





Input Loading Factors
$\overline{CLOCK}$, $\overline{SET}$ = 1.75
J, K, = 0.75

Output Loading Factor = 10

J-K TRUTH TABLE

Typical Characteristics
(V_{CC} = 5.0 V; T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz typ
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd+} = 12 ns
t_{pd-} = 12 ns

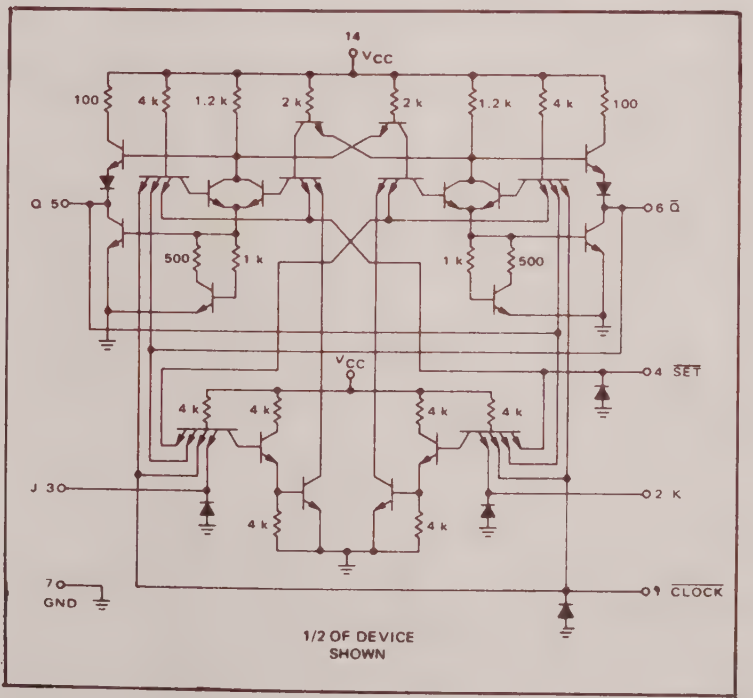


FIGURE 4-33

CIRCUIT TYPE MC4044F, L, P

PHASE-FREQUENCY DETECTOR

INPUT STATE	INPUT RI	INPUT VI	OUTPUT U1	OUTPUT D1	OUTPUT U2	OUTPUT D2
1	0	0	X	X	1	1
2	1	0	X	X	0	1
3	1	1	X	X	1	0
4	1	0	X	X	0	1
5	0	0	X	X	1	1
6	1	0	X	X	0	1
7	0	0	X	X	1	1
8	1	0	X	X	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

1 X indicates output state unknown

2 U1 and D1 outputs are sequential i.e. they must be sequenced in order shown

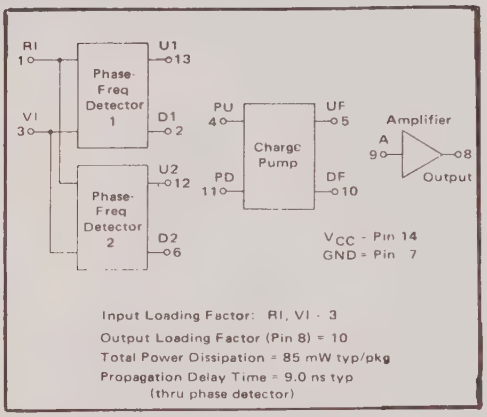
3 U2 and D2 outputs are combinational, i.e. they need only inputs shown to obtain outputs

This device contains two digital phase detectors and a charge pump circuit which converts MTTL inputs to a dc voltage level for use in frequency discrimination and phase-locked-loop applications

The two phase detectors have common inputs. Phase-frequency detector 1 is locked in (indicated by both outputs high) when the negative transitions of the variable input (VI) and reference input (RI) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, the U1 (up) output goes low; conversely the D1 (down) output goes low when the variable input is higher in frequency or leads the reference input in phase. It is important to note that the duty cycles of the variable input and the reference input are not important since negative transitions control system operation.

Phase detector 2, on the other hand, is locked in when the variable input phase lags the reference phase by 90° (indicated by the U2 and D2 outputs alternately going low with equal pulse widths). If the variable input phase lags by more than 90°, U2 will remain low longer than D2, and, conversely, if the variable input phase lags the reference phase by less than 90°, D2 remains low longer. In this phase detector the variable input and the reference must have 50% duty cycles

The charge pump accepts the phase detector outputs (U1 or U2 applied to PU, and D1 or D2 applied to PD) and converts them to fixed amplitude positive and negative pulses at the UF and DF outputs respectively. These pulses are applied to a lag-lead active filter, which incorporates external components, as well as the amplifier provided in the MC4344/4044 circuit. The filter provides a dc voltage proportional to the phase error



Input Loading Factor: RI, VI - 3

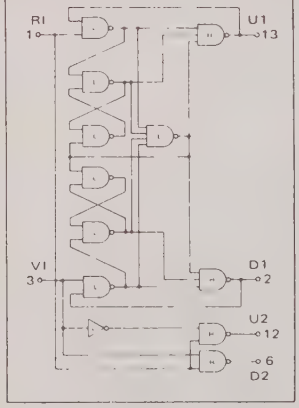
Output Loading Factor (Pin 8) = 10

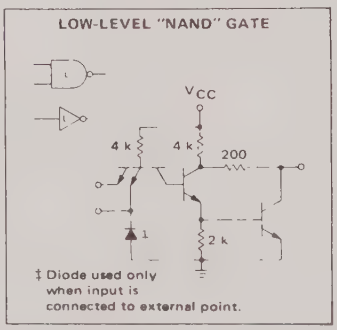
Total Power Dissipation = 85 mW typ/pkg

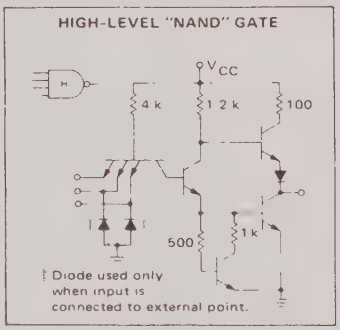
Propagation Delay Time = 9.0 ns typ (thru phase detector)

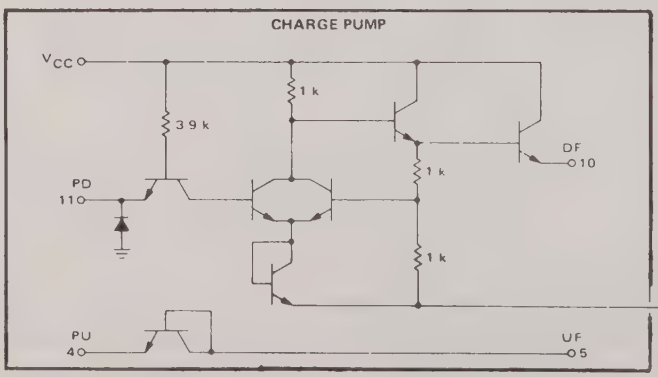
PHASE DETECTOR

The phase detector portion of this device is constructed using low and high-level gates interconnected as shown by the logic diagram









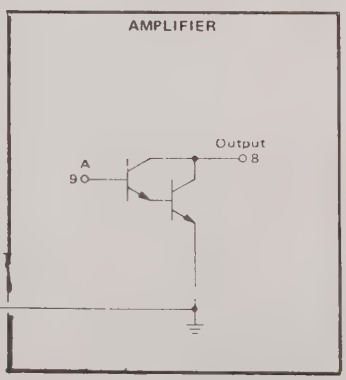


FIGURE 4-34

CIRCUIT TYPE MC10131 MC10231

DUAL TYPE D MASTER-SLAVE FLIP-FLOP

R-S TRUTH TABLE

R	S	Q^{n+1}	$\bar{Q}^{n+1}$
L	L	Q^n	$\bar{Q}^n$
L	H	H	L
H	L	L	H
H	H	N.D	N.D

N.D. = Not Defined

SEQUENTIAL TRUTH TABLE

D	C	$\bar{C}_E$	Q_{n+1}
L	L	L	Q_n
L	L	H	L
L	H	L	Q_n
L	H	H	Q_n
H	L	L	Q_n
H	L	H	H
H	H	L	Q_n
H	H	H	Q_n

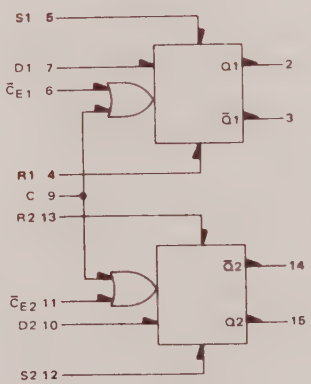
The MC10131 is a dual master-slave type D flip-flop. Asynchronous set (S) and reset (R) override clock (C) and clock enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the clock enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

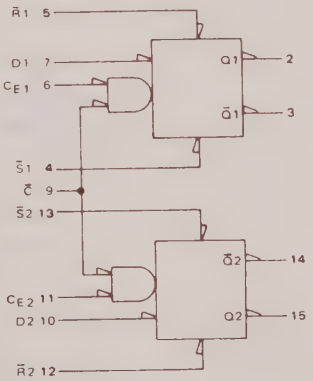
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

P_D = 225 mW typ/pkg
f_{Tog} = 160 MHz typ

POSITIVE LOGIC



NEGATIVE LOGIC



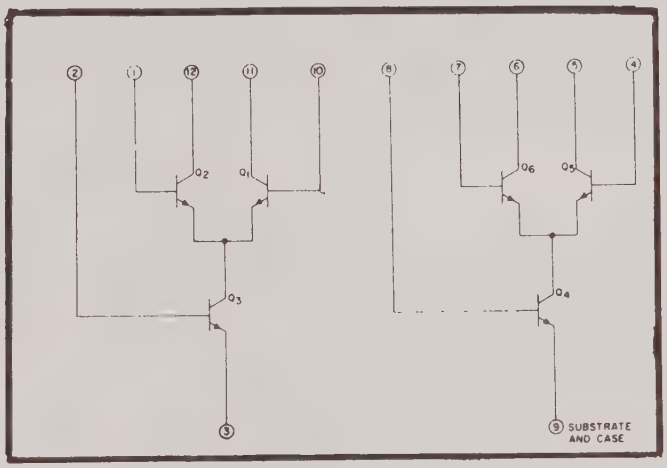
V_{CC1} - Pin 1
V_{CC2} - Pin 16
V_{EE} - Pin 8

FIGURE 4-35

CIRCUIT TYPE CA3049

Dual Independent Differential RF/IF Amplifier

Input Bias Current	10	μA	typ.
Collector-Cutoff Current	100	nA	max.
Collector-to-Emitter Breakdown Voltage	15	V	min.
Insertion Power Gain at 200MHz	23	dB	typ.
Noise Figure at 200MHz	4.6	dB	typ.



12-lead TO-5

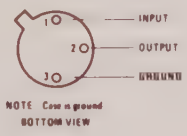
FIGURE 4-36

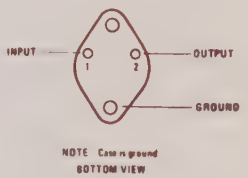
CIRCUIT TYPE LM109, 209, 309(K)
5 VOLT MONOLITHIC REGULATOR

The LM109, LM209 and LM309 are complete 5V monolithic regulators. They are designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The devices are easy to use, minimize the number of external components, and are available in two common transistor packages. In the solid-kovar TO-5 header, they can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC's from overheating. If internal dissipation is too great, the regulators switch on and off with a duty cycle that prevents excessive heating.

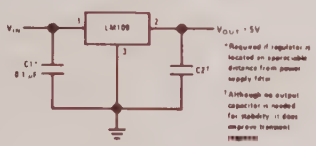
The LM109, LM209 and LM309 do not use a zener diode for the internal reference. Instead, the reference is developed from the highly-predictable emitter-base voltage of the transistors. This unique low-voltage reference makes possible operation with input voltages below 6.5V. Further, production tolerances are tight enough that individual adjustment is unnecessary. It is a simple matter to guarantee worst case output voltages under all conditions, including variations in temperature, input voltage and load as well as long term stability, that are well within the operating range of digital logic.



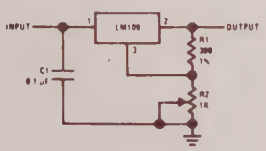


Typical Applications

Fixed 5V Regulator



Adjustable-Output Regulator



Current Regulator

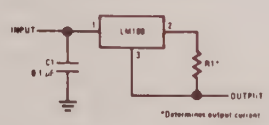


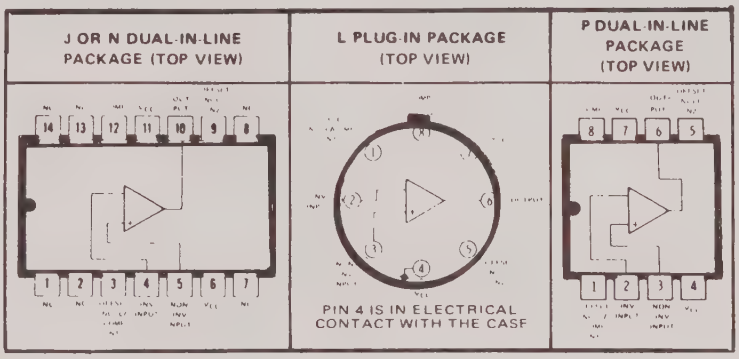
FIGURE 4-37

CIRCUIT TYPES LM301AN, SN52101A, SN72301A
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

The SN52101A and SN727301A are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make the SN52101A and SN72301A ideal for voltage-follower applications. The devices are protected to withstand short-circuits at the output. The external compensation of the SN52101A and the SN72301A allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate.

A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 8, to null out the offset voltage.


J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)
L PLUG-IN PACKAGE (TOP VIEW)
P DUAL-IN-LINE PACKAGE (TOP VIEW)
14 13 12 11 10 9 8
1 2 3 4 5 6 7
8 7 6 5
1 2 3 4
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC—No internal connection

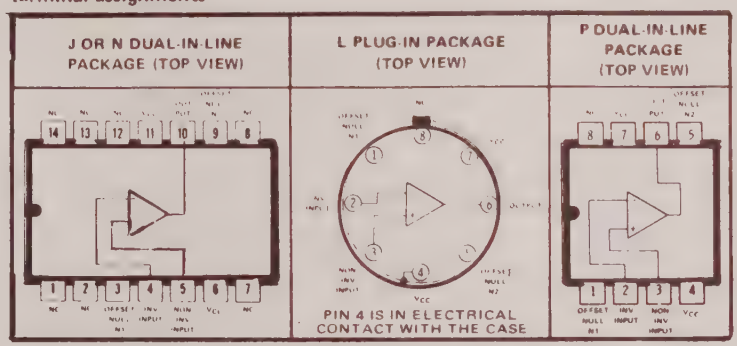
FIGURE 4-38

CIRCUIT TYPES LM307, SN52107, SN72307
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

The SN52107 and SN72307 are high-performance operational amplifiers, featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

The high common-mode input voltage range and the absence of latch-up make the SN52107 and SN72307 ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset-null inputs,

terminal assignments


J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)
L PLUG-IN PACKAGE (TOP VIEW)
P DUAL-IN-LINE PACKAGE (TOP VIEW)
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

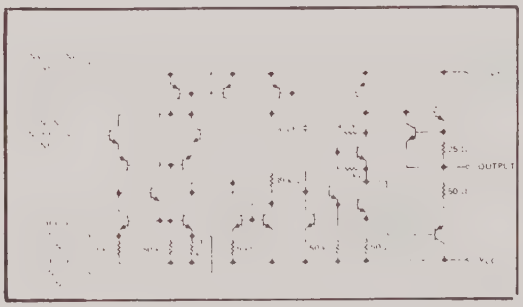
NC - No internal connection

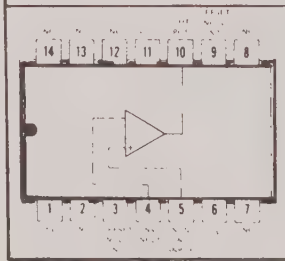
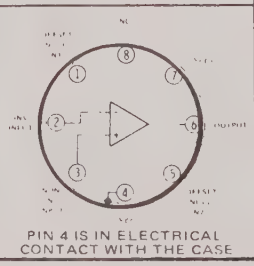
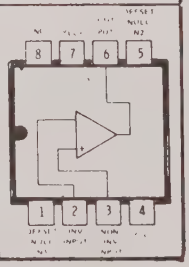
FIGURE 4-39

CIRCUIT TYPES LM471 SN52741
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage

schematic



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)	L PLUG-IN PACKAGE (TOP VIEW)	P DUAL-IN-LINE PACKAGE (TOP VIEW)
		

PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

NC--No internal connection

FIGURE 4-40

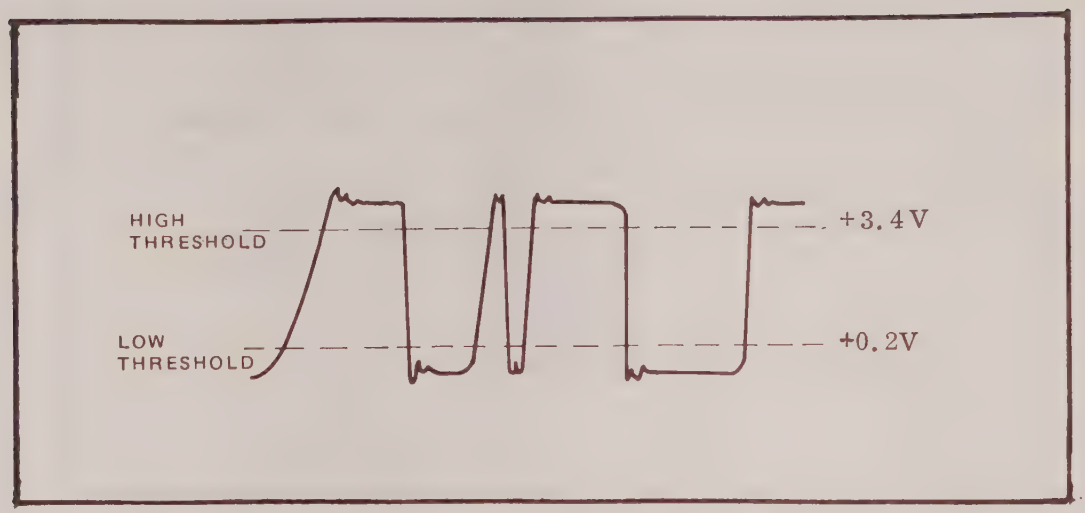


FIGURE 4-41
TYPICAL TTL DIGITAL SIGNAL

Figure 4-41 shows a typical Transistor-Transistor-Logic (TTL) signal. The relative value of a signal voltage with respect to the threshold voltages determines the operation of the circuit. A signal greater than the high threshold is in the high state and its actual voltage whether it's +4 volts or +5 volts is unimportant to the operation of the circuit. The above oscilloscope wave form displays absolute voltage with respect to time, but in digital electronics the absolute value is unimportant. A digital signal exists in one of three states - high, low and undefined or between levels - each determined by a threshold voltage. It is the relative value of the signal voltage with respect to these thresholds that determines the logic state of the signal and the operation of the IC. As indicated in Figure 4-41 if the signal is greater than +3.4 volts, it is at a high state and it is unimportant what its absolute level is. Similarly for a low state the voltage must be below +0.2 volts.

Within each digital logic family, such as TTL, RCL, ECL, the timing characteristics of each component are well defined. Each gate displays a characteristic propagation delay time, rise time, and fall time. The effects of these timing parameters on circuit operation are taken into account by the design engineer. Once a design has been developed beyond breadboard or prototype stage and is into production, problems due to design have been resolved. An important characteristic of digital IC's is that when they fail, they fail catastrophically. This means that timing parameters rarely degrade or become marginal. Thus, observing on an oscilloscope and making repeated decisions on the validity of timing parameters is time consuming, and contributes very little, if any, to the troubleshooting process. The fact that pulse activity exists is usually enough indication of proper IC operation without further observation of pulse width, repetition rate, rise time or fall time.

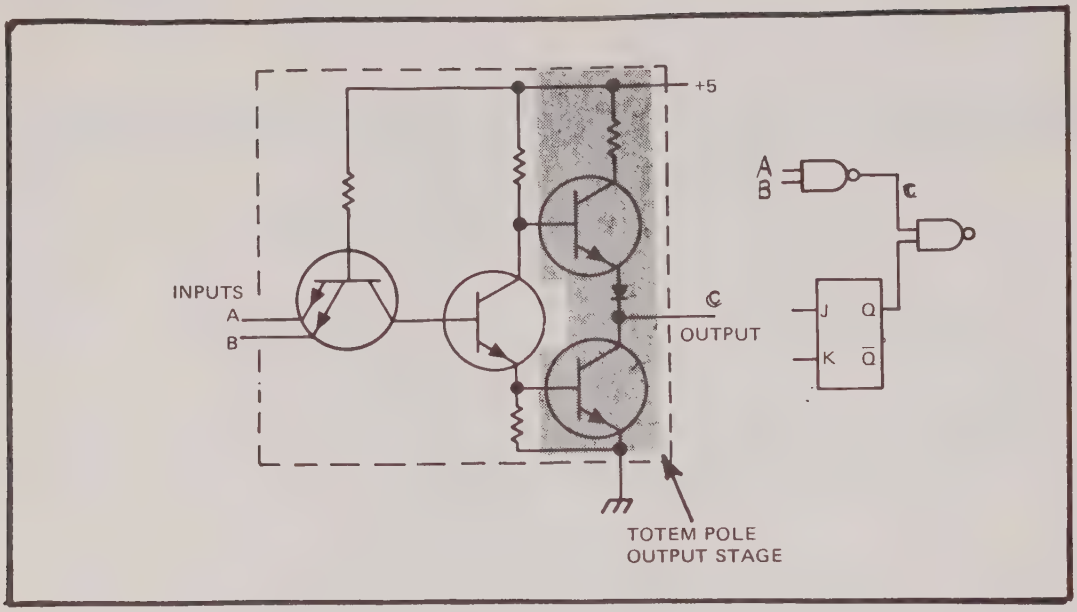


FIGURE 4-42

OUTPUT "TOTEM POLE" CONFIGURATION OF A TTL IC

Figure 4-42 shows a problem created by the TTL logic family. The output stage of a TTL device is a transistor totem pole. In either the high or low state, it has a low impedance output. In the low state it is a saturated transistor to ground. It thus appears as 5-10 ohms to ground. This presents a problem to in-circuit stimulation. A signal source used to inject a pulse at a node which is driven by a TTL output must have sufficient power to override the low impedance output state.

Thus, the use of the traditional oscilloscope and the traditional signal sources is inefficient. Since the diodes and transistors are packaged in the IC, use of diode checkers is also marginal. These tools are general purpose tools that can be applied to any situation if the troubleshooter has enough time. But with the quantity and complexity of today's electronic circuits, it makes sense to find the most efficient solution to the problem at hand. This suggests using the oscilloscope diode checkers and voltmeter on discrete circuits, and using logic state analysis, Boolean equations and Truth Tables on digital IC circuitry.

In order to troubleshoot efficiently, it is important to understand the type of failures found in digital circuits. These can be categorized into two main classes--those caused by a failure internal to an IC and those caused by a failure in the circuit external to the IC.

There are five basic types of failures that can occur internally in the IC.

1. An open bond on either the input or output.

2. A short between the input or output and V_{CC} or ground.

3. A short between two pins (neither of which is V_{CC} or ground).

4. A failure in the internal steering logic of the IC.

5. A failure of an active logic function within the IC.

In addition to the five internal types of failures, there are four types of failures that can occur in the circuit external to the

IC, these are:

1. A short between a node and V_{cc} or ground
2. A short between two nodes (neither of which are V_{cc} or ground).
3. An open signal path.
4. A failure of discrete component.

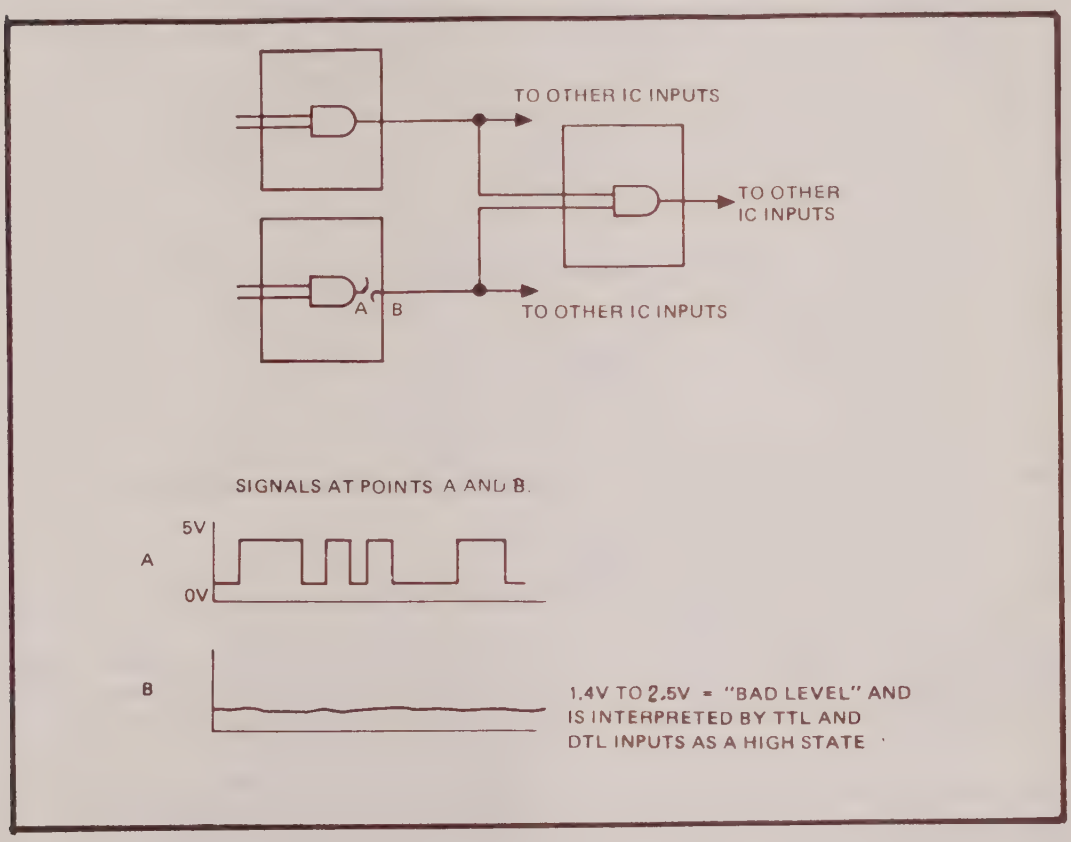


FIGURE 4-43
THE EFFECT OF AN OPEN BOND UPON CIRCUIT OPERATION

Before discussing how to detect these failures we will discuss the effect they have upon circuit operation. The first failure internal to an IC mentioned was an open bond on either an input or output. This failure has a different effect depending upon whether it is an open output bond or an open input bond. In the case of an open output bond (Figure 4-43), the inputs driven by that output are left to float. In TTL and DTL circuits a floating input rises to approximately 1.4 to 2.5 volts and usually has the same effect on circuit operation as a high logic level. Thus, an open output bond will cause all inputs driven by that output to float to a true level since 2.5 volts is less than the high threshold level of 3.4 volts and greater than the low threshold level of .2 volt. In TTL and DTL logic, a floating input is interpreted as a high level.

A short between an input or output and V_{cc} or ground has the effect of holding all signal lines connected to that input or output either high (in the case of short V_{cc}) or low (if shorted to ground) (Figure 4-44). This will cause signal activity at points beyond the short to disappear and thus this type of failure is catastrophic in terms of circuit operation.

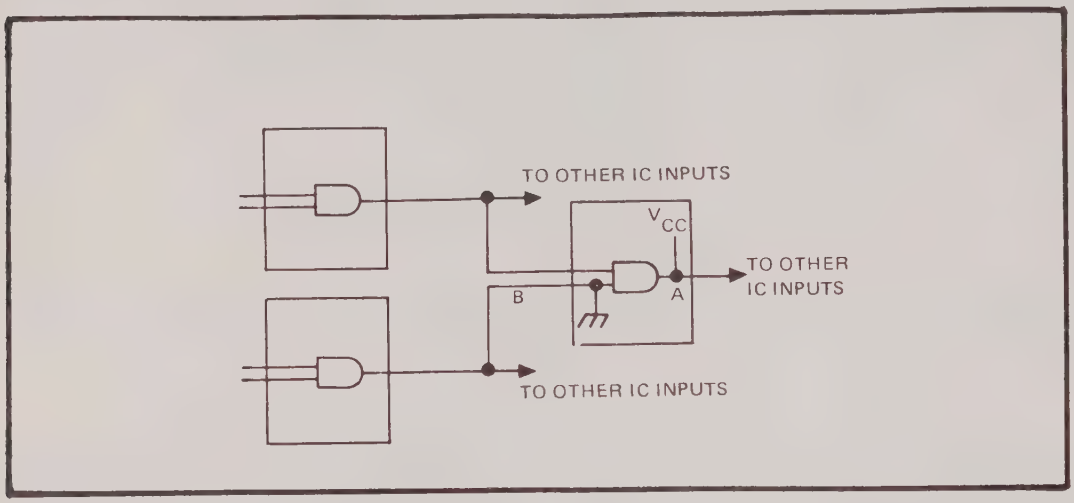


FIGURE 4-44

THE EFFECT OF A SHORT BETWEEN AN INPUT OR OUTPUT AND V_{cc} OR GROUND

All signal lines connected to point A are held in the high state. All signal lines connected to point B are placed at a low state.

A short between two pins is not as straightforward to analyze as a short to V_{cc} or ground. When two pins are shorted the outputs driving those pins oppose each other (Figure 4-45). In this situation the output attempting to go high will draw current through the upper saturated transistor of its totem pole output stage while the output attempting to go low will sink through the saturated lower transistor of its totem pole output stage. The net effect is that the short will be pulled to a low logic level by the saturated transistor to ground. Whenever both outputs attempt to go high simultaneously or to go low simultaneously, the shorted pins will respond properly.

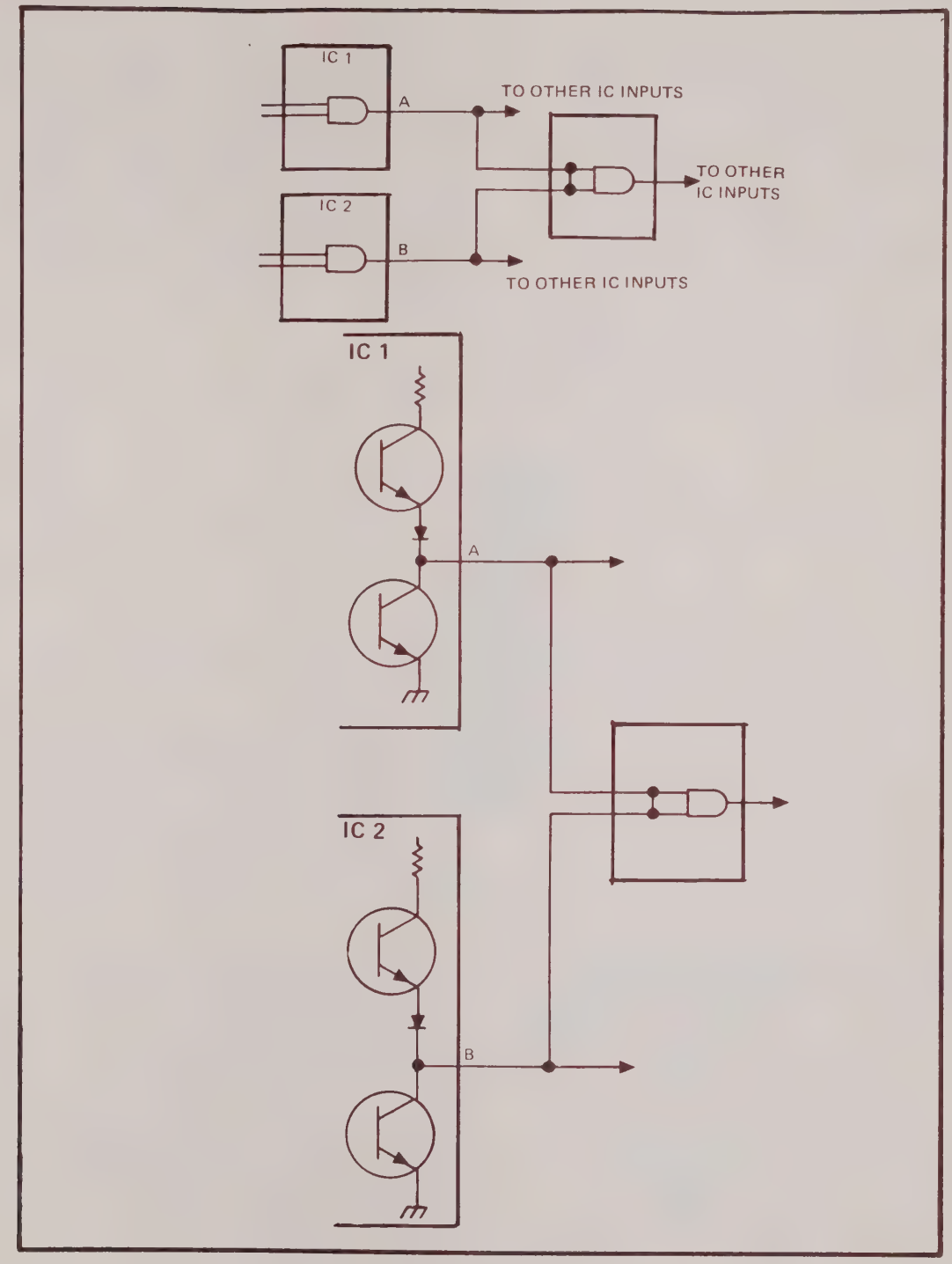


FIGURE 4-45

SHORT BETWEEN TWO PINS

The error effect of a short between two pins occurs when the outputs driving those pins attempt to pull the short to opposite states. In this case the output attempting to pull the node high will be supplying current, while the output attempting to pull the node low is a saturated transistor to ground, and will be sinking the current. The saturated transistor to ground will pull the node to a low state.

The fourth failure mode internal to an IC is the failure of the internal steering logic of the IC (Figure 4-46). This has the effect of permanently turning on the upper transistor of the output totem pole configuration thus locking the output at a logic high state or turning on the lower transistor thus locking the output to a low logic state. This type of failure blocks the signal flow and has a catastrophic effect upon the circuit operation.

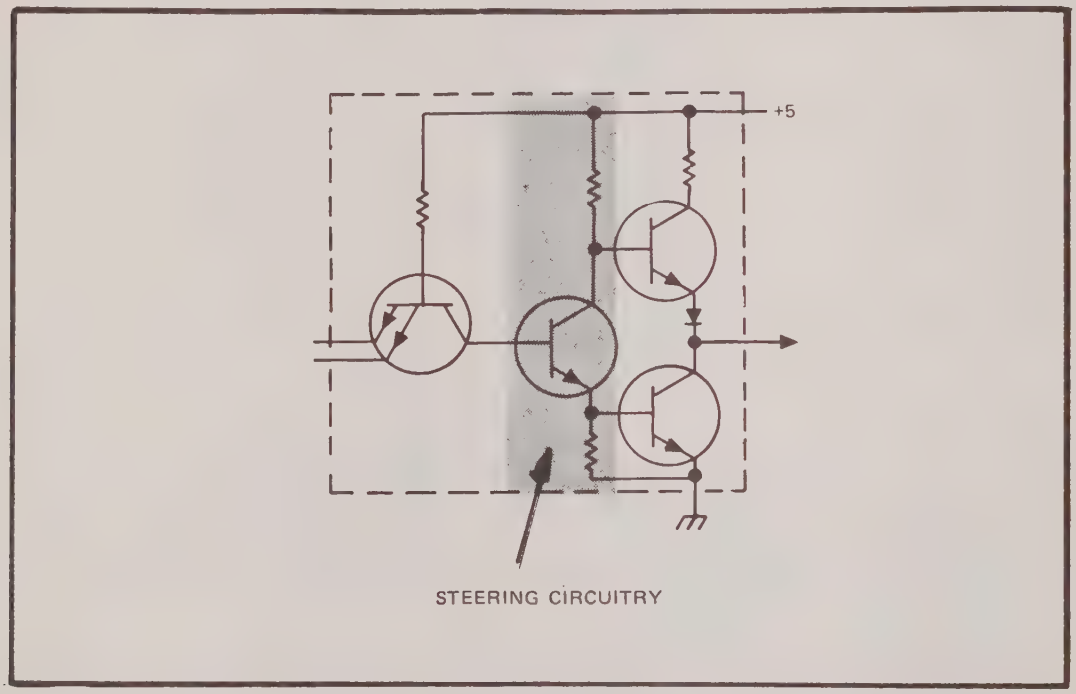


FIGURE 4-46

THE EFFECT OF A FAILURE OF INTERNAL STEERING LOGIC OF AN IC

A short between a node and V_{cc} or ground external to the IC is indistinguishable from a short internal to the IC. Both will cause the signal lines connected to the node to be either always high (for shorts to V_{cc}) or always low (for shorts to ground). When this type of failure is encountered only a very close examination of the circuit will reveal if the failure is external or internal to the IC.

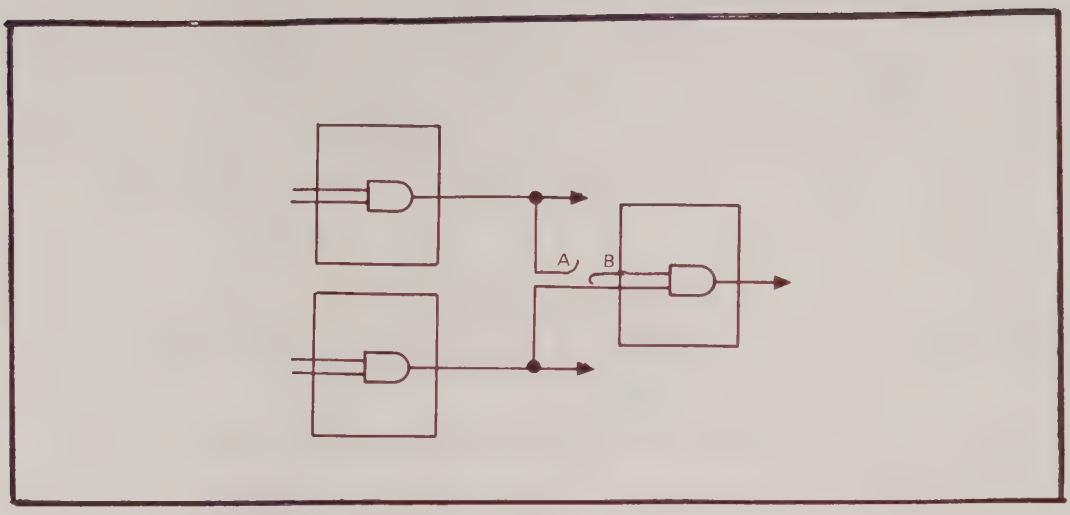


FIGURE 4-47

THE EFFECT OF AN OPEN IN A CIRCUIT EXTERNAL TO AN IC

An open signal path in the circuit has an effect that is similar to the effect of an open output bond driving the node. (Figure 4-47) All inputs attached to the node at point A will be driven properly. All input to the right of the (open point B) will float and thus appear as a logic high.

4.4.4 General Counter Troubleshooting

When the Counter fails to operate in all ranges the cause of the malfunction is related to one or more of the following functional assemblies:

1. Input Processor and 1st DCU PCB Assembly A1A2.
2. Counter Display PCB Assembly A2.
3. Power Supply PCB Assembly A3.
4. Reference Oscillator Assembly A7.
5. Clock Control Assembly A6.

Table 4-10 outlines the procedure to sectionalize and isolate the fault to an individual assembly or circuit function when the counter does not operate in any of the three ranges.

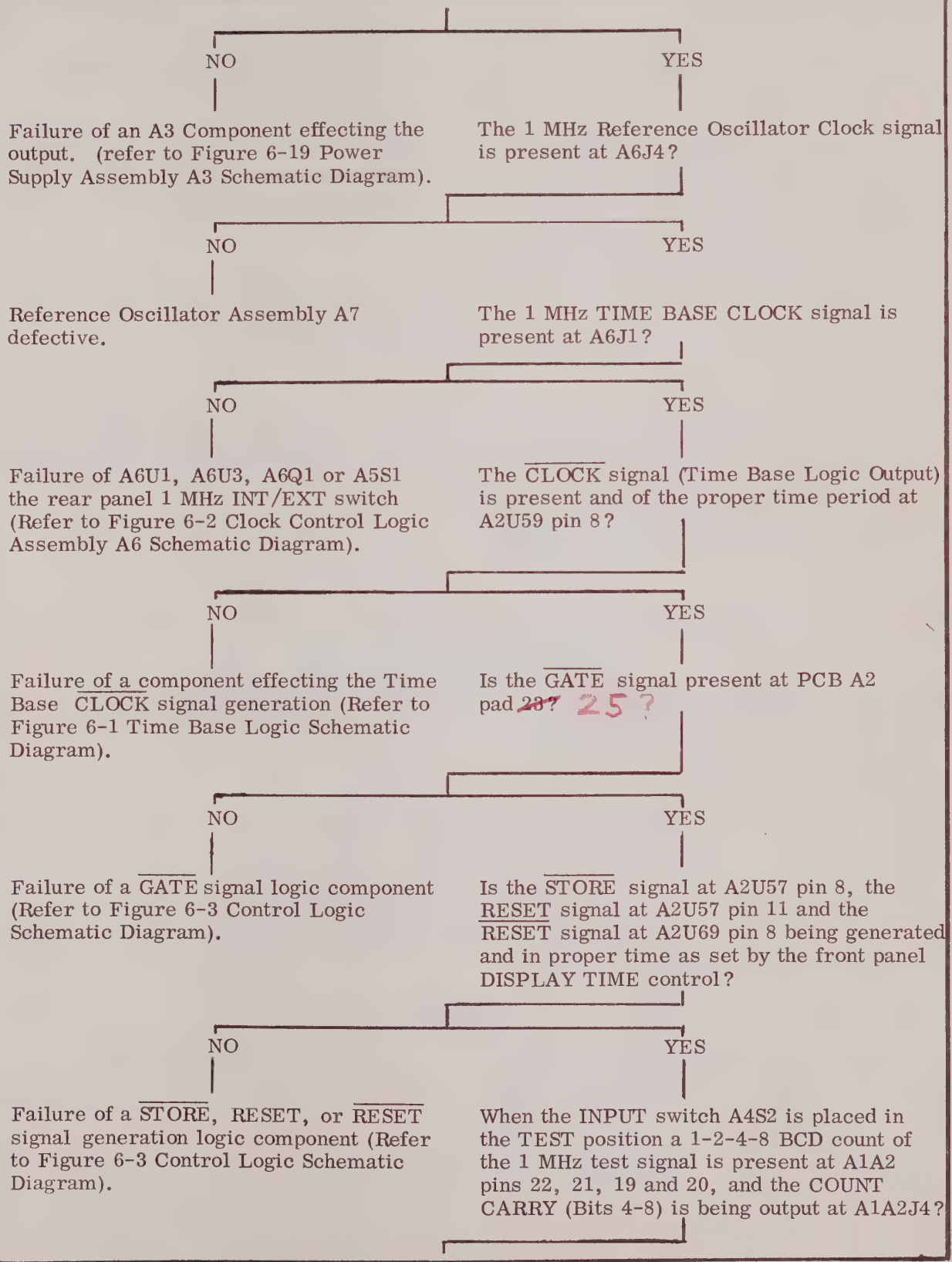
TABLE 4-10

GENERAL COUNTER SECTIONALIZATION AND LOCALIZATION TROUBLESHOOTING CHART

Counter does not operate in any range

Are the proper voltages present at the following pads of the Power Supply Assembly A3?

A3 PAD NO. (S)	OUTPUT
3	+190 V unregulated
4	+190 V ground return
1	+28 V unregulated
2	+28 V ground return
13	+18 V regulated
12	+18 V ground return
9 & 10	+12 V regulated
5	-12 V regulated
6, 7, & 8	±12 V ground return
U	+5 V unregulated
T	+5 V ground return
11	+5 V regulated
20 & 21	+5 V regulated
18 & 19	-5.2 V regulated
14, 15, 16 & 17	±5 V ground return


NO
YES
Failure of an A3 Component effecting the output. (refer to Figure 6-19 Power Supply Assembly A3 Schematic Diagram).
The 1 MHz Reference Oscillator Clock signal is present at A6J4?
NO
YES
Reference Oscillator Assembly A7 defective.
The 1 MHz TIME BASE CLOCK signal is present at A6J1?
NO
YES
Failure of A6U1, A6U3, A6Q1 or A5S1 the rear panel 1 MHz INT/EXT switch (Refer to Figure 6-2 Clock Control Logic Assembly A6 Schematic Diagram).
The CLOCK signal (Time Base Logic Output) is present and of the proper time period at A2U59 pin 8?
NO
YES
Failure of a component effecting the Time Base CLOCK signal generation (Refer to Figure 6-1 Time Base Logic Schematic Diagram).
Is the GATE signal present at PCB A2 pad 23? 25?
NO
YES
Failure of a GATE signal logic component (Refer to Figure 6-3 Control Logic Schematic Diagram).
Is the STORE signal at A2U57 pin 8, the RESET signal at A2U57 pin 11 and the RESET signal at A2U69 pin 8 being generated and in proper time as set by the front panel DISPLAY TIME control?
NO
YES
Failure of a STORE, RESET, or RESET signal generation logic component (Refer to Figure 6-3 Control Logic Schematic Diagram).
When the INPUT switch A4S2 is placed in the TEST position a 1-2-4-8 BCD count of the 1 MHz test signal is present at A1A2 pins 22, 21, 19 and 20, and the COUNT CARRY (Bits 4-8) is being output at A1A2J4?

NO

Failure of the input gate control IC-NOR gate A1A2U3A. Failure of an IC in the 1st DCU circuit A1A2U3B, U4 or U5. Failure of the ECL to TTL translators A1A2U6. Failure of the CARRY Gate and Translator circuit A1A2Q1, 2, 3 or 4. (Refer to Figure 6-7 Input Processor and 1st DCU PCB Assembly Schematic Diagram).

YES

When the INPUT switch A4S2 is placed in the TEST position and the RESOLUTION/ BLANKING switch A4S3 is placed in the 1 Hz position the Display reads 00 001 000 000.

NO

Failure of a Count Chain component, Strobe Display Logic component, or Visual Display component (Refer to Figures 6-4 and 6-5 the Count Chain Schematic Diagram and the Strobed Display Logic Schematic Diagram).

YES

When the RESOLUTION/BLANKING switch is placed in the 10 Hz position, the LSD of the display (the Units digit) is blanked?

NO

Failure of A2U72, A2U73 element C, A2Q11 or A4S3 switching selection (Refer to Figure 6-5 Strobed Display Logic Schematic Diagram).

YES

When the RESOLUTION/BLANKING switch is placed in the 100 Hz position, the two LSD's of the display are blanked?

NO

Failure of A2U72, A2U73 element C, and D A2Q10, A2Q11 or A4S3 switching selection, (Refer to Figure 6-5 Strobed Display Logic Schematic Diagram).

YES

When the RESOLUTION/BLANKING switch is placed in the 1 kHz position, the three LSD's of the display are blanked?

NO

YES

Failure of A2U72, A2U73 element C, D, A2U76 element C, A2Q9, A2Q10, A2Q11 or A4S3 switching Selection (Refer to Figure 6-5 Strobed Display Logic Schematic Diagram).

When the RESOLUTION/BLANKING switch is placed in the 10 kHz position the four LSD's display are blanked?

NO

Failure of A2U72, A2U73 elements C, D, A2U76 element C, D, A2Q8, A2Q9, A2Q10, A2Q11 or A4S3 switching selection.

4.4.5 Troubleshooting the Counter on a Range 1 Fault or Failure

When the counter fails to count or provides an incorrect count in Range 1 operation and the operation on Range 2 and 3 is normal, the cause of the malfunction is related to the Range 1 input amplifier or the gate input selection. circuits, and thus is isolated to the A1A1 and A1A2 PCB plug in assemblies.

Table 4-11 outlines the procedure to sectionalize, and localize the fault to an individual functional circuit or component part, when the counter indicates a Range 1 malfunction.

TABLE 4-11

RANGE 1 MALFUNCTION

SECTIONALIZATION AND LOCALIZATION TROUBLESHOOTING CHART

Counter malfunctions in Range 1

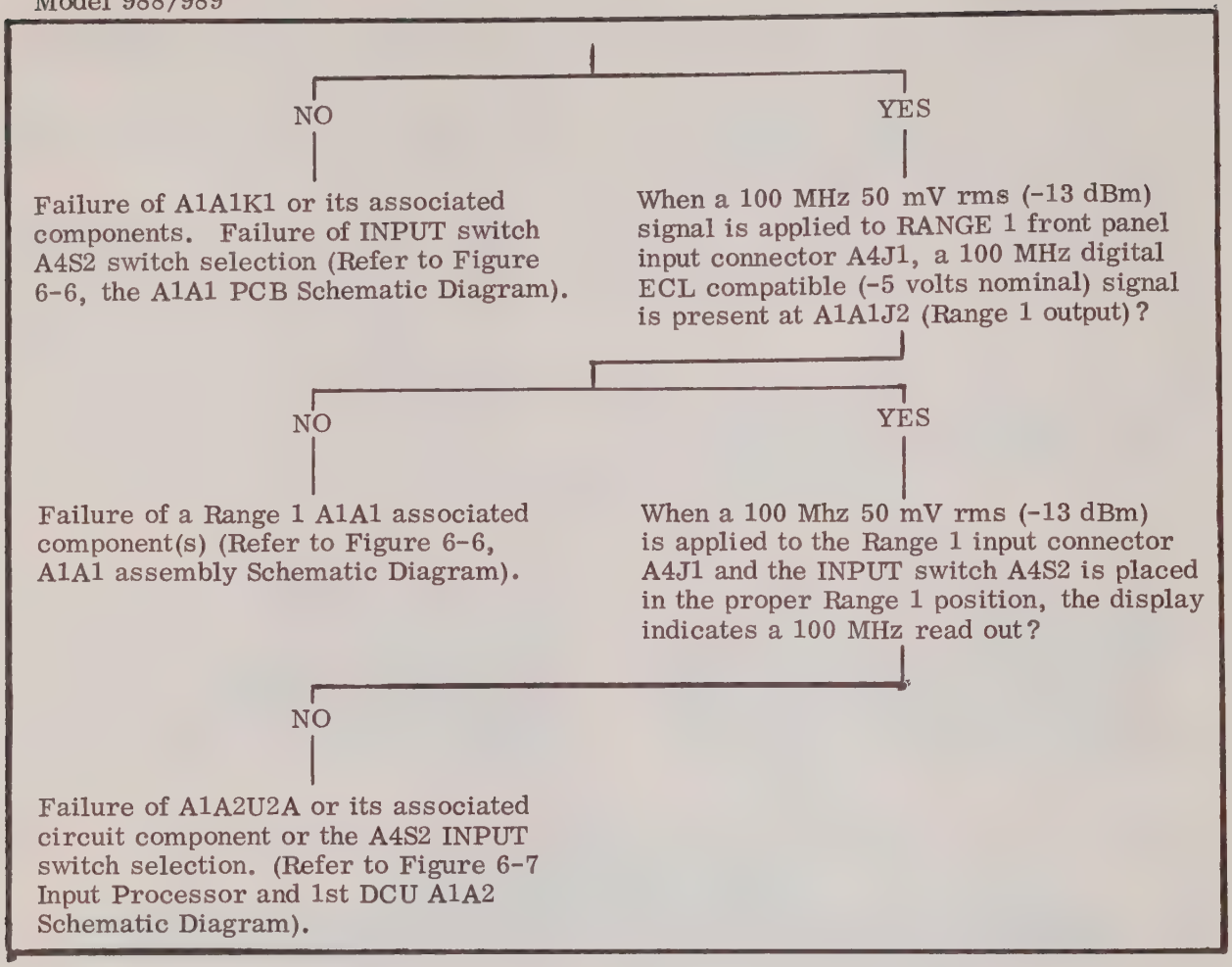
Is the Range 1 Input Amplifier Threshold Adjustment A1A1R4 properly set (Refer to the Range 1 Input Amplifier Threshold Adjustment Procedure Paragraph 4.3.3, page 4-5 of this manual)?

NO

Perform the Range 1 Input Threshold Adjustment Procedure (Table 4-3, page 4-5).

YES

When the INPUT switch A4S2 is switched from the RANGE 1 50Ω position to the RANGE 1 1MΩ position, the input amplifier input impedance is configured from 50Ω to 1MΩ?


NO
YES
Failure of A1A1K1 or its associated components. Failure of INPUT switch A4S2 switch selection (Refer to Figure 6-6, the A1A1 PCB Schematic Diagram).
When a 100 MHz 50 mV rms (-13 dBm) signal is applied to RANGE 1 front panel input connector A4J1, a 100 MHz digital ECL compatible (-5 volts nominal) signal is present at A1A1J2 (Range 1 output)?
NO
YES
Failure of a Range 1 A1A1 associated component(s) (Refer to Figure 6-6, A1A1 assembly Schematic Diagram).
When a 100 Mhz 50 mV rms (-13 dBm) is applied to the Range 1 input connector A4J1 and the INPUT switch A4S2 is placed in the proper Range 1 position, the display indicates a 100 MHz read out?
NO
Failure of A1A2U2A or its associated circuit component or the A4S2 INPUT switch selection. (Refer to Figure 6-7 Input Processor and 1st DCU A1A2 Schematic Diagram).

4.4.5 Troubleshooting the Counter on a Range 2 Fault or Failure

When the Counter Malfunctions in Range 2 operation and the operation is normal in Range 1 and 3, the malfunction is related to the Range 2 Input Amplifier or the divide by four prescaler located on assembly A1A1 or the Range 2 Input control gate A1A2U2.

Table 4-12 outlines the procedure to sectionalize and localize the malfunction of a Range 2 associated circuit or component part.

TABLE 4-12

RANGE 2 MALFUNCTION

SECTIONALIZATION AND LOCALIZATION TROUBLESHOOTING CHART

Counter Malfunctions when in Range 2 operation.

When a 625 MHz 100 mV rms (-7 dBm) signal is applied to the RANGE 2 input connector A4J2 a 625 MHz ECL compatible (-5 volts nominal) signal is present on the collectors of A1A1Q7 and A1A1Q8? (Refer to Figure 6-1, the A1A1 Schematic Diagram).

NO

1. Failure of the Range 2 input amplifiers A1A1Q5 or A1A1Q6 or their associated circuit components.
2. Failure of the steering transistors A1A1Q7 or A1A1Q8 or their associated components. (Refer to Figure 6-1, the A1A1 assembly Schematic Diagram).

YES

When a 625 MHz 100 mV rms (-7 dBm) signal is applied to the Range 2 front panel input connector a 312.5 MHz -5 Volt nominal signal is present at A1A1U2 pin 7.

NO

Failure of a ÷ 2 circuit transistors A1A1Q9 thru A1A1Q25 or its associated passive components. (Refer to Figure 6-1, A1A1 assembly Schematic Diagram).

YES

With a 625 MHz 100 mV rms (-7 dBm) signal applied to the Range 2 front panel input connector, a 156.25 MHz -5 Volt nominal signal is present at A1A1J4.

NO

Failure of A1A1U2, A1A1R35, A1A1R34 or A1A1C32 (Refer to Figure 6-1, A1A1 assembly Schematic Diagram.

YES

When a 625 MHz 100 mV rms (-7 dBm) is applied to the front panel and the INPUT switch is placed in the RANGE 2 position, the display indicates 625 MHz.

NO

1. Failure of A1A2 U2 element B or its associated passive components.

2. Failure of INPUT switch Range 2 select generating the RANGE 2 ENABLE signal (Refer to Figure 6-2 the A1A2 assembly Schematic Diagram).

4.4.7 Troubleshooting the Model 988/989 Counter with a Range 3 Malfunction

When the Model 988/989 Counter malfunctions in Range 3 operation and the operation in Range 1 and 2 is normal, the malfunction is related to a fault in the Auto Het function. The assemblies and components that are allied to the Auto Het function are A1A3 thru A1A15 and the "plumbing" (RF semi-ridged coax cables) and other interfacing components. Due to the complexity of the Auto Het function, and the interreaction of sub-functions and functional loops, the troubleshooting procedures must involve the observation and malfunction isolation of the sub-group functions and their interfaces as the proper troubleshooting technique. Another problem is that the substitution method is not practical in the case of the Hybrid "T" (A1A14), the Back Diode Detector (A1A15) or the YIG tuned Multiplier (A1A8), because of their high dollar value.

The functional sub-groupings of the Auto Het function as applied to the troubleshooting techniques are listed as follows, and each is supported by a separate troubleshooting chart or procedure.

1. Start Detection, and RF Input Function (Table 4-13)

2. Stop Detection and IF Amplifier Function (Table 4-14)

3. 200 MHz YIG Drive Generation Function (Table 4-15

4. Sweep Generation Function (Table 4-16)

5. Preset "N" Number Generation Function (Table 4-17)

6. D/A Converter Function (Table 4-18)

7. YIG Tuned Multiplier and Ramp Drive Function

TABLE 4-13

START DETECTION AND RF
INPUT FUNCTION TROUBLESHOOTING CHART

With a 3 GHz 0 dBM (200 mV rms) signal applied to the Range 3 input "N" type connector, the INPUT LEVEL meter (A4M1) indicates half scale deflection?

NO YES

Is the START command signal present at A1A1U11, pin 6?

NO

1. Perform the Range 3 Input Meter Calibration procedure, Steps 1 thru 4 of Table 4-4.
2. Check the Input Level Meter circuit A1A4Q1, U12 and its associated circuit components. (Refer to Figure 6-9 the A1A4 Assembly Schematic Diagram).
3. Check the Start Detector Take Off circuit located in the IF Amplifier Assembly A1A13. The components that make up this circuit consists of A1A13L1, C3 and C1 (Refer to Figure 6-18 the A1A13 Assembly Schematic Diagram).
4. Check the Back Diode Detector A1A15.

CAUTION

Maximum reverse current of the diode is 10mA and its video resistance (Rv is in the order of 100Ω, thus when checking front-to-back resistance with a VOM insure that the x 100 or greater range is used.

5. Check the Hybrid "T" A1A14 and the "RF plumbing" that interfaces the Hybrid "T" with the input connector and the Back Diode Detector.
6. Check the front panel Range 3 input "N" type connector A4J3 (This connector has a 3 dB attenuator pad built into its assembly.)

YES

1. Check for a $\overline{\text{RANGE 3 ENABLE}}$ signal as a logic low at A1A4 pin J. 2. Check the INPUT switch A4S2 for the proper Range 3 enable function (ground selected). 3. Check the Start Detector circuit consisting of A1A4Q2, U11, R6 thru R11, C2 and CR1. (Refer to Figure 6-9 the A1A4 Assembly Schematic Diagram).	Normal operation.

TABLE 4-14

STOP DETECTOR AND IF AMPLIFIER

FUNCTION TROUBLESHOOTING PROCEDURE

If the Counter does not lock on to a Range 3 input signal that is within the proper frequency range, and of the proper level due to a Stop command signal malfunction, perform the following procedure.

STEP	ACTION
1	Perform the Stop Dectector Alignment procedure presented in Table 4-5.
2	Check the IF Amplifier A1A13J2 output for the presence of a correct IF signal using the test configuration in steps 1 thru 4 of Table 4-5.
3	Troubleshoot the IF Amplifier Assembly A1A13 (Refer to Figure 6-18 the A1A13 Assembly Schematic Diagram).
4	Check the Stop Detector circuit components located in Assembly A1A7 using the following isolation procedure with reference to Figure 6-12 the A1A7 Schematic Diagram. a. If step 5 of the alignment procedure Table 4-4 did not provide a correct display read out the malfunction is in the IF Shaper Circuit. b. If steps 6 thru 10 of the alignment procedure Table 4-4 did not provide the correct action the malfunction is within the In Band Detector circuit.

Table 4-14 Stop Detector and IF Amplifier Function Troubleshooting Procedure (Continued)

	c. If step 11 of Table 4-4 did not provide the correct action the malfunction is in the Reset Detector circuit. d. If step 12 of Table 4-4 did not provide the correct action the malfunction is in the Threshold Detector circuit. e. If the $\overline{\text{LOCK}}$ command at A1A7 pin 6, the D/A STOP command at A1A7 pin A or the $\overline{\text{STOP}}$ command at A1A7 pin 1 is not present, the malfunction is due to a failure of the One-Shot Reset M.V., the Start-Stop R-S flip-flop or the associated gating circuits (these circuits are shown to the left of the test points TP1, TP2, TP3 as illustrated in Figure 6-12 A1A7 Assembly Schematic Diagram.

TABLE 4-15

200 MHz YIG DRIVE FUNCTION TROUBLESHOOTING PROCEDURE

The 200 MHz YIG Drive signal must be referenced to the 1 MHz Reference Oscillator and have the proper drive level, and spectral purity (side band rejection) if proper operation of the YIG is to be maintained. If the 200 MHz YIG Drive signal is suspected, perform the following troubleshooting procedure.

STEP	ACTION
1	Check the 1 MHz Phase Lock Clock signal applied to the 20 MHz Phase Lock Oscillator Assembly input connector A1A12J2. If it is not present or out of tolerance the malfunction is the Phase Lock Clock Buffer A6U3, element A, located in the Clock Control Assembly A6 (Refer to Figure 6-2 assembly, A6 Schematic Diagram).
2	Perform the 20 MHz Phase Lock Oscillator Adjustment Procedure Table 4-6, if the adjustment procedure does not correct the malfunction, the problem is in the 20 MHz Phase Lock Oscillator Assembly A1A12. (Refer to Figure 6-17 A1A12 Assembly Schematic Diagram.
3	Perform the 200 MHz Frequency Multiplier Alignment Procedure Table 4-7. If the alignment of the 200 MHz Frequency Multiplier did not correct the malfunction, troubleshoot the A1A11 circuitry (Refer to Figure 6-16 A1A11 Assembly Schematic Diagram).
4	Check the 200 MHz Power Amplifier A1A9, the Power Level Adjustment control A1R2, the Power Level Control Transistor A1Q2.

Table 4-15 200 MHz YIG Drive Function Troubleshooting Procedure (Continued)

5	Adjust the YIG Drive Level Control A1A16R17 and the Power Level Control for proper YIG drive.
6	Check the YIG Controller Circuit located on PCB Assembly A1A6 (Refer to Figure 6-11 A1A6 assembly Schematic Diagram)

TABLE 4-16

SWEEP GENERATION FUNCTION TROUBLESHOOTING PROCEDURE

If the Sweep Generator fails to generate a digital output sweep or it does not generate a sweep covering the full range for the proper ramp development, perform the following troubleshooting procedure.

STEP	ACTION
1	Extend the Sweep Generator PCB Assembly A1A3 on an extender board.
2	Disconnect the coax cable from the IF input connector on the Stop Detector PCB A1A7J1 to prevent generation of a $\overline{\text{STOP}}$ command by the Stop Detector Logic.
3	Apply a 3 GHz signal to the Range 3 input connector A4J3, and adjust its level for a midscale indication on the front panel LEVEL meter A4M1.
4	With an oscilloscope monitor the Digital Sweep's 10^{-1} Bit "1" output at the PCB connector pin J (A1A3-J) a pulse train should be present. If no pulse activity is present check the following circuit test points to isolate the failure. a. A1A3U11 pin 11 (Output of the 1st Sweep Counter) should have a pulse activity of approximately 6 kHz. b. A1A3Q2 collector (Sweep oscillator output) should have a pulse activity of $\simeq$ 50 kHz. c. A1A3U3 pin 8 (Sweep start/stop gate) should have a logic low state (0 volts).
5	Monitor the Digital Sweep's 10^{-1} Bit "8" at A1A3-P for proper pulse activity if not present, a failure of A1A3U13 the 10^{-1} Sweep Counter IC is indicated.

Table 4-16 Sweep Generation Function Troubleshooting Procedure (Continued)

6	Monitor the Digital Sweeps 10^0 Bit "8" at A1A3-L for proper pulse activity, if not present a failure of A1A3U14 is indicated.
7	Monitor the Digital Sweeps 10^1 Bit "8" at A1A3-S for proper pulse activity, if not present a failure of A1A3U12 is indicated.
8	Monitor the Digital Sweeps 10^2 Bit "2" at A1A3-11 for proper pulse activity, if not present a failure of A1A3U10 is indicated.
9	Monitor A1A3U5 pin 6 with an oscilloscope, a 5 microsecond gate at a ≃ 1 second rate should be present, if not a failure of the Reset One-Shot M. V. consisting of A1A3U5 element C, A1A3Q3, C6, R12 and R13 or the Reset NAND gate A1A3U3 element C is indicated.
10	Reconnect the coax cable to the IF input A1A7J1 and verify that the Digital Sweep will lock on (Stop), on the presence of a $\overline{\text{STOP}}$ command signal, if it does not lock on a failure of A1A3U3 or A1A3U1 element E is indicated.

TABLE 4-17
PRESET "N" NUMBER GENERATION
FUNCTION TROUBLESHOOTING PROCEDURE

If the Model 988/989 Counter does not display the Preset "N" number on the three most significant digits of the front panel's visual display or an incorrect number is displayed, the malfunction is related to the Preset "N" Number Generation Function located on PCB assembly A1A4. Table 4-17 provides the trouble-shooting procedure to isolate the fault or failure. If one or more of the three most significant digits does not illuminate, perform all steps of the procedure. If the malfunction provides an incorrect readout of the three most significant digits of the visual display perform steps 6 thru 9 of the procedure.

STEP	ACTION
1	Extend the A1A4 PCB assembly with an extender board, apply power to the Counter and select Range 3 operation.
2	Apply a 13.4 GHz signal to the Range 3 input connector and adjust the signals level for a midscale indication on the Counter's INPUT LEVEL meter.
3	Monitor A1A4U4 pin 12 with an oscilloscope for a 500 kHz clock signal. If the 500 kHz clock is not present a 1A4U4 IC failure is indicated.

Table 4-17 Preset "N" Number Generation Function Troubleshooting Procedure (Continued)

4	With an oscilloscope monitor A1A4U1 pin 8 while depressing the Counter's manual RESET front panel push button switch, after each Auto Het lock on cycle, a 500 kHz clock should gate on upon the release of the push button switch, and gate off upon a Auto Het lock on. If the 500 kHz clock does not gate on when the RESET push button is released a failure of A1A4U5 element A or the reset circuit of A1A4U4 is indicated. If the problem is not a reset function and the 500 kHz clock does not gate on when the $\overline{\text{STOP}}$ command signal is present, the malfunction is due to a A1A4U1 gate failure or a A1A4U5 element B failure.
5	With an oscilloscope monitor the following signals, while depressing the Counter's manual RESET push button switch after each Auto Het lock on cycle, the absence of pulse activity or an incorrect count rate will indicate a failure related to the IC being monitored. A1A4U2 pin 9 — 125 kHz A1A4U2 pin 8 — 62.5 kHz A1A4U2 pin 11 — 31.25 kHz A1A4U3 pin 12 — 15.62 kHz A1A4U3 pin 9 — 7.81 kHz A1A4U3 pin 8 — 3.90 kHz A1A4U3 pin 11 — 1.95 kHz A1A4U4 pin 9 — 975 Hz
6	Change the frequency of the applied test signal to 7.8 GHz and readjust its level for a midscale indication on the INPUT LEVEL meter. Verify if the three most significant digits (MSD) of the visual display reads 078, (if it does not, make note of the fact).
7	Change the frequency of the applied signal to 8.10 GHz and verify that the three MSD's of the visual display reads out 081 (if it does not, make note of the fact).
8	Change the frequency of the applied signal to 10.70 GHz and verify that the three MSD's of the visual display reads out 107 (if it does not, make note of the fact).
9	If the visual display did not indicate the correct readings of the three MSD's in steps 6 thru 8, the malfunction is related to the "N" Number Stop Comparator circuit configured by IC's A1A4U6, U7, &9 and U10. By referring to Figure 6-9 the A1A4 assembly Schematic Diagram and monitoring with an oscilloscope the exclusive OR gates and the Hex Inverters outputs, the fault can be isolated to the IC element that is malfunctioning.

TABLE 4-18
D/A CONVERTER FUNCTION TROUBLESHOOTING PROCEDURE

If the Model 988/989 will not operate properly due to a ramp generation failure or malfunction related to the D/A converter function perform the following trouble-shooting procedure to isolate the fault or failure to a circuit element or component.

STEP	ACTION
1.	Extend the A1A5 PCB assembly with an extender board, apply power to the counter and select Range 3 operation. Check the + 3.10 V reference voltage at PCB A1A5 pin 17. If not present or out of tolerance a malfunction of the reference voltage regulator circuit is indicated, check the following components. 1. A1A5Q1 Series regulator. 2. A1A5U4 IC Amplifier. 3. A1A5CR1 Reference Zener. 4. A1A5R44 thru R49. 5. A1A5C1 thru C4.
2.	Remove the coax cable from A1A7J1 to disable the generation of a $\overline{\text{STOP}}$ command and input a valid Range 3 test signal of 3 GHz at a level to provide midscale deflection on the INPUT LEVEL meter.
3.	Monitor A1A5 pin B or 2 with an oscilloscope a negitive going step ramp of ≈+ 8 volts amplitude should be present. If no ramp is present a failure of A1A5U5 (Summation Amplifier) is indicated.
4.	If the ramp is present at A1A5 pin B and 2, but has a "glitch" (drops a step or jumps a step proceed with the following procedure. On a dual trace Oscilloscope display the step ramp on trace "A" and monitoring the following transistor bases on trace "B" with the Oscilloscope triggered on the ramp signal leading up clock.

POINT OF TEST	INDICATION	COMPONENT (S) AT FAULT
A1A5Q1-base	No 10^{-1} Bit "1" pulse	A1A5U3, R4
A1A5-pin B	No ramp step	A1A5Q1, R1, R2, R3
A1A5Q2-base	No 10^{-1} Bit "2" pulse	A1A5U3, R8
A1A5-pin B	No ramp step	A1A5Q2, R5, R6, R7

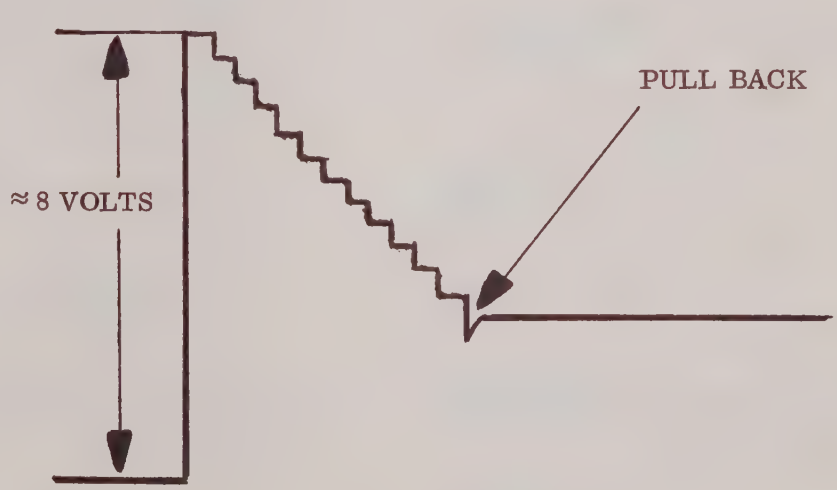
TABLE 4-18
D/A CONVERTER FUNCTION TROUBLESHOOTING PROCEDURE
Continued

	POINT OF TEST	INDICATION	COMPONENT (S) AT FAULT
	A1A5Q3-base	No 10^{-1} Bit "4" pulse	A1A5U3, R12
	A1A5-pin B	No ramp step	A1A5Q3, R9, R10, R11
	A1A5Q4-base	No 10^{-1} Bit "8" pulse	A1A5U2, R16
	A1A5-pin B	No ramp step	A1A5Q4, R13, R14, R15
	A1A5Q5-base	No 10^{0} Bit "1" pulse	A1A5U2, R18
	A1A5-pin B	No ramp step	A1A5Q5, R17
	A1A5Q6-base	No 10^{0} Bit "2" pulse	A1A5U2, R20
	A1A5-pin B	No ramp step	A1A5Q6, R19
	A1A5Q7-base	No 10^{0} Bit "4" pulse	A1A5U1, R22
	A1A5-pin B	No ramp step	A1A5Q7, R21
	A1A5Q8-base	No 10^{0} Bit "8" pulse	A1A5U2, R24
	A1A5-pin B	No ramp step	A1A5Q8, R23
	A1A5Q9-base	No 10^{1} Bit "1" pulse	A1A5U3, R26
	A1A5-pin B	No ramp step	A1A5Q9, R25
	A1A5Q10-base	No 10^{1} Bit "2" pulse	A1A5U3, R28
	A1A5-pin B	No ramp step	A1A5Q10, R27
	A1A5Q11-base	No 10^{1} Bit "4" pulse	A1A5U1, R30
	A1A5-pin B	No ramp step	A1A5Q11, R29
	A1A5Q12-base	No 10^{1} Bit "8" pulse	A1A5U1, R32
	A1A5-pin B	No ramp step	A1A5Q12, R31
	A1A5Q13-base	No 10^{2} Bit "1" pulse	A1A5U1, R34
	A1A5-pin B	No ramp step	A1A5Q13, R33
	A1A5Q14-base	No 10^{2} Bit "2" pulse	A1A5U1, R36
	A1A5-pin B	No ramp step	A1A5Q14, R35
	A1A5Q17-base	No 10^{-2} Bit "1" pulse	A1A5U2, R54
	A1A5-pin B	No ramp step	A1A5Q17, R51, R52, R53
	A1A5Q18-base	No 10^{-2} Bit "2" pulse	A1A5U2, R58
	A1A5-pin B	No ramp step	A1A5Q18, R55, R56, R57
	A1A5Q19-base	No 10^{-2} Bit "4" pulse	A1A5U1, R62
	A1A5-pin B	No ramp step	A1A5Q19, R59, R60, R61

TABLE 4-18
D/A CONVERTER FUNCTION TROUBLESHOOTING PROCEDURE
Continued

	POINT OF TEST	INDICATION	COMPONENT (S) AT FAULT
	A1A5Q20-base A1A5-pin B	No 10^{-2} Bit "8" pulse No ramp step	A1A5U3, R66 A1A5Q20, R63, R64, R65

STEP	ACTION
5.	Reconnect the coax cable to A1A7J1 that was disconnected in Step 2, with a 3 GHz test signal applied to the range 3 input monitor A1A5-pin B noting the sweep ramp at its stop time, the sweep ramp should stop stepping and pull back (go more positive) to a level that is less than one step in amplitude. Refer to the following wave form.



STEP	ACTION
5. (Continued)	If the ramp does not pull back adjust R38 fully CW, manually reset the counter and recheck the ramp at its stop level for the pull down effect. If pull down is not noted a failure of A1A5Q16, R39, R38, or R39 is indicated.

YIG DRIVER AND CONTROLLER FUNCTION TROUBLESHOOTING PROCEDURE.

The function of the YIG Driver and Power Amplifier Controller Assembly A1A6 is to supply the proper drive to the YIG tuning coil and to control the gain of the 200 MHz Power Amplifier. If the YIG Tuned Multiplier does not output the proper frequency or its output veries in amplitude check the YIG coil drive signal or the controller leveling signal, for proper operation with an oscilloscope.

4.5 REPAIR AND COMPONENT REPLACEMENT TECHNIQUES

Repair of the Microwave Counter should be undertaken only by personnel qualified in solid state repair techniques. When a component failure is encountered, observe these general instructions:

1. Remove power before removing a PC board or any component.
2. Use only a grounded, transformer-coupled, thermostatically controlled soldering iron.
3. Use a heat-sink when required to prevent thermal damage to PC board pads and tracing interconnect wiring and solid state components.
4. Avoid application of acid-core solder, clean solder connection surfaces with approved solvent or alcohol-water solution.

4.5.1 POWER TRANSISTOR REPLACEMENT

In the event that transistor A1Q1 or A1Q2 mounted on the Auto Het Chassis fails, proceed as follows:

1. Remove wire connections from each lead of the defective transistor.
2. Remove the hardware securing the transistor to the mounting.
3. Coat both sides of the mica washer with heat conducting grease (Dow Corning compound 107 or equivalent).
4. Align the mica washer with the hole in the Auto Het Chassis and install the replacement transistor with the exposed metallic portion toward the mica washer. Secure the transistor in place with the existing hardware.
5. Solder the wire connections to the leads of the transistor.

4.5.2 INTEGRATED CIRCUIT REPLACEMENT

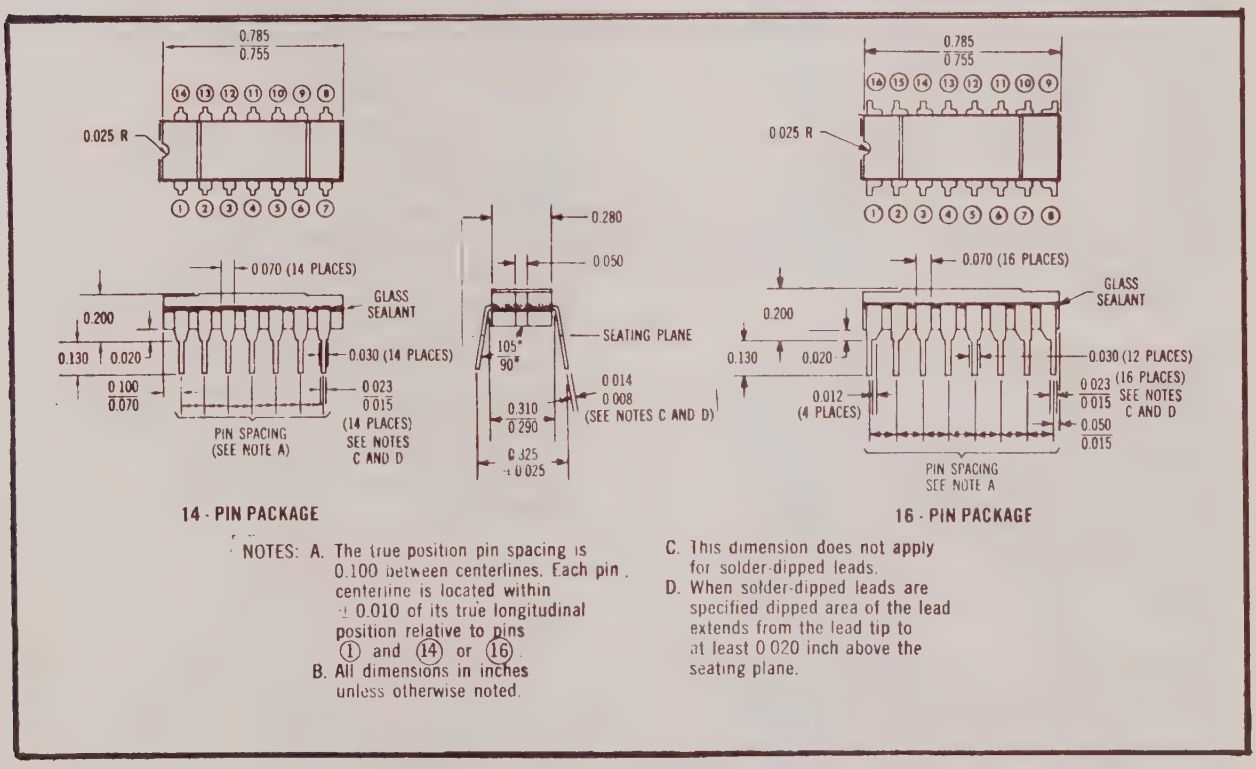
The following instruction outline the proper method for the removal and replacement of a defective IC dual-inline-package.

1. Verify that the IC is defective (refer to the Integrated Circuit Data Sheets of the particular IC to analyze its failure or defective internal circuit).
2. At the component side of the PC board, carefully clip each lead of

the defective IC at the point where the lead enters the case package.

3. Carefully remove each individual lead from the component side of the PC board with the aid of a soldering iron and long nose pliers.
4. Remove all excess with a pneumatic solder extractor.
5. Install the replacement IC noting correct orientation of the index notch as depicted by the respective component location illustration.
6. Solder each lead on the circuit side and all top pads on the component side of the PC board.

Most IC's used in the Model 988/989 are packaged in the standard dual-inline-package (DIP). These packages utilize 300-mil row spacing and 100-mil lead spacing. Thus if the proper replacement is used, alignment of the DIP should present no problem. An index notch allows for the proper orientation and the adaptation of a insertion/heat sink tool. The late series Model 988/989 (-6) provides IC DIP sockets on the A2 PCB assembly for the 77 IC's located on this assembly. Figure 4-48 provides the demensional characteristics of the DIP IC's.



NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins ① and ⑭ or ⑯.
B. All dimensions in inches unless otherwise noted.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

FIGURE 4-48
IC DIP DEMENSIONS AND TOLERANCES

4.5.3 UHF and SHF Component Repair Techniques

The assemblies utilized in the GHz range consist of the YIG Tuned Multiplier A1A8, the Hybrid Coupler A1A14, the Back Diode Detector A1A15 and the semi ridged coax cables. These devices are none-repairable so no special repair techniques are required, other than care in connecting the 3 millimeter SMA type connectors, to prevent damage to the coax line and/or connectors.

Since the GHz internal circuit components are physically small so not to become resonant in the operating range, thermal time constants are small. So these devices are easily damaged by pulse inputs such as static discharge or residual line charges. The Hybrid Coupler and the Back Diode Detector can be damaged if a input greater than +20 dBm (2.2 Vrms) is applied to the Range 3 input connector.

Components that operate in the 600 MHz range are located on PCB A1A1, the Range 2 Prescaler consists of 19 Micro-miniature MMT3960 type high speed switching transistors. These devices are physically very small (less than .092 inches in diameter) and can be easily damaged physically or thermally if not handled properly.

The under side of the A1A1 PCB has a V_{ee} plane. This is <u>not</u> a ground plane, and is at - 5.2 volts and if shorted to ground will "take down" the - 5.2 volt power supply. The Prescaler ground plane is located on the upper (component) side of the PCB and care should be taken when replacing a MMT3960 type transistor to prevent shorting to the ground plane. To keep leads as short as possible and allow collector-to-collector and emitter-to-emitter connection, transistors A1A1Q10, Q12, Q13, Q15, Q18, and Q23 are mounted in an inverted position (white dot down), and when replaced must be orientated in the inverted position.

Circuit components that operate in the 200 MHz range are located within the 200 MHz Frequency Multiplier A1A11, the 200 MHz Power Amplifier A1A9 and the IF Amplifier A1A13 assemblies. These assemblies present special problems in the areas of repair, component replacement and troublshooting.

The 200 MHz Assemblies consists of PCB packaged inside aluminum containers to assure circuit RF isolation (shielding). These circuits will not operate properly if the cover is removed from the shielded inclosers. This makes trouble shooting by scoping or voltage measurement difficult is not impossible. When a component is replaced assure that it is orientated in the same position as the component that was removed, to prevent changing the distributed L and C values of the circuit. The lumped inductances of the circuits are provided for by coils fabricated out of turns of 20 AWG buss wire, these inductors must not be reoriented or disturbed physically as to turn spacing or turn diameter, because it would change both the lumped and distributed L and C values of the circuit and drastically effect circuit operation.

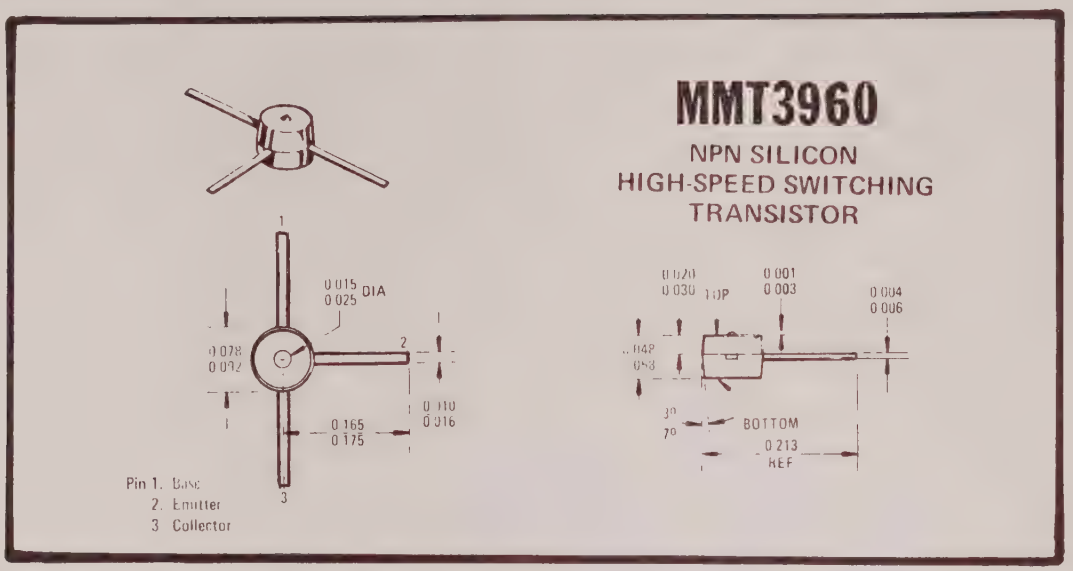


FIGURE 4-49
MMT3960 TRANSISTOR, OUTLINE,
DEMENSIONAL, AND ORIENTATIONAL DATA

SECTION 5
PARTS LIST

5.1 GENERAL

This section contains the required information for ordering replacement parts from Eldorado Instruments commercial sources or from Department of Defense (when a military part number is provided).

To use the part lists, first refer the schematic and component location diagram in Section 6 to identify the part as to its reference designation number which is an alphanumerical group that consists of a basic reference designation, that prefixes all reference designations that apply to the subassembly or assemblies within which the item is located, including those of the highest level needed to designate the items uniquely. For example:

Read from right to left as: First resistor (R1) of third subassembly (A3) of the first assembly (A1).

Class Designation Letters, are in accordance with USAS Standard Y32-16-1968, Reference Designations for Electrical and Electronic Parts and Equipments. The following class designations are used within the Model 988/989 are listed alphabetical with definitions of the class letter (s).

A. . . .Assembly, separable and/or repairable.
C. . . .Capacitor, (F) (E)
CR. . .Diode, Semiconductor device
DS . . .Lamp, incandescent
E. . . .Part, miscellaneous, (E)
F. . . .Fuse, (F)
FL. . .Filter, (E)
J. . . .Connector, receptacle, (F) (E)
L. . . .Inductor, (F) (E)
M . . .Meter, counter (F) (E)
P. . . .Connector, plug (F) (E)
Q. . . .Transistor
R. . . .Resistor, Potentiometer
S. . . .Switch
T. . . .Transformer (F) (E)
U. . . .Integrated Circuit Package
V. . . .Tube, electronic (Display)
X. . . .Socket (F), single item mounting, always used as a prefix in a composite class designation, ie; XV, XA
Y. . . .Crystal unit (F)

(F) Function
(E) Electrical

When the reference designator has been determined refer to the proper assembly parts list to obtain the required ordering information, which includes the component description and values, the manufacture's code, the part number and the EE part number.

Table 5-1, provides a cross reference from the Manufacture's Code, which is the two-to-four letter code in the part list Mfg. column, to the manufacture's name and address, also provided is the Federal Supply Code for Manufacture's (FSCM).

5.2 ORDERING INFORMATION

To order replacement parts from Eldorado, address all order or inquiries directly to:

CUSTOMER SERVICE PARTS DEPT.
Eldorado Instruments Company
2495 Estand Way
Pleasant Hill, California 94523
(415) 682-2100

When ordering, specify the following information for each part:

a. Instrument Model and Serial Number.

b. Complete part description including: The assembly designation, part

designation and part number/s (Mfgr's and Eldorado's).

5.3 NUMERICAL INDEX

A numerical index of the part numbers is provided and is formated in four columns. Column 1 contains the manufactures or MIL part number in alpha-numerical arrangement sequence (alphabetic O's are listed as numeric zeros). Column 2 contains the Federal Supply Code for Manufactures (FSCM). Columns 3 and 4 contain the goverment-assigned codes for source, maintenance and recoverability (SMR).

TABLE 5-1
MANUFACTURE'S CODE-TO-MANUFACTURE

MFG. CODE	MANUFACTURE'S NAME AND ADDRESS	FSCM
AB	Allen-Bradley Co., Milwaukee, Wisconsin	01121
AER	Aertech Ind., Sunnyvale, California	21847
AMI	Amercon Microwave Ind., Waltham Massachusetts	
AML	Amphenol Electronics Corp., Broadview, Illinois	02660
AMPE	Amperex Electronics Corp., Hicksville, New York	28092
AVAN	Avantek Inc., Santa Clara, California	24539
BECK	Beckman Instruments, Helipot Div., Fullerton, California	05721
BRNS	Bourns, Inc., Riverside, California	51641
BUR	Burroughs Corp., Plainfield, New Jersey	83594
CAM	Cambridge Thermionic Corp., Cambridge, Massachusetts	71279
CDC	Continental Device Corp., Hawthorne, California	07910
CEC	Component Engineering Co., Chicago, Illinois	22666
CH	Cutler Hammer Inc., Milwaukee, Wisconsin	15605
CK	C & K Components, Inc., Newton Massachusetts	09353
CRL	Centralab, Milwaukee, Wisconsin	71590
CTS	Chicago Telephone Supply, Elkart, Indiana	71450
DEL	Delevan Electronics Corp., Augora, New York	99800
EI	Eldorado Instruments Co., Pleasant Hill, California	54495
ELC	ELCO Corp., Philadelphia, Pennsylvania	91662
ERR	Erie Technological Products, Erie, Pennsylvania	72982
FAI	Fairchild Semiconductor, Mountain View, California	13715
FILT	Filtaire, Inc., Charlottesville, Virginia	21689
GE	General Electric Co., Auburn, New York	09214
HPA	Hewlett Packard Associates, Palo Alto, California	28480

TABLE 5-1
MANUFACTURE'S CODE-TO-MANUFACTURE
(Continued)

MFG. CODE	MANUFACTURE'S NAME AND ADDRESS	FSCM
IDC	International Diode Corp., Jersey City, New Jersey	16068
IEC	International Electronic Corp., Melville, L.I., New York	24138
IMB	IMB Electronic Products, Santa Fe Springs, California	27556
ITT	ITT Semiconductors, West Palm Beach, Florida	14433
LICN	Licon Division, Illinois Tool Works, Inc., Chicago, Illinois	04426
LTTL	Littelfuse, Inc., Des Plaines, Illinois	75915
MOT	Motorola, Phoenix, Arizona	04713
NAT	National Electronics, Inc., Geneva, Illinois	83781
NBX	Nobex Division of Griffith Plastic Products Co., Burlingame, California	32767
OMNI	Omniyig Inc., Palo Alto, California	
OVEN	Overaire, Inc., Charlottesville, Virginia	12020
RAY	Raytheon Corp., Waltham, Massachusetts	49956
RCA	RCA, Harrison, New Jersey	99089
SAN	Sangamo Electric Co., Springfield, Illinois	53021
SEAL	Sealectro, Mamroneck, New York	98291
SEM	Semtech Corp., Newbury Park, California	14099
SOL	Solitron Devices, Riviera Beach, Florida	95077
SPR	Sprague Electric, North Adams, Massachusetts	01884
STA	Stackpole Carbon Co., St. Mary's, Pennsylvania	78488
SWT	Switchcraft, Inc., Chicago, Illinois	82398
TI	Texas Instruments, Dallas, Texas	01295
VER	Vernitron Electric Company, Lakeport, New Hampshire	10651
VIS	Vishay Resistor Prod., Malvern, Pennsylvania	18612
WAK	Wakefield Engineering Inc., Wakefield, Massachusetts	05820

NUMERICAL INDEX

PART NUMBER	FSCM	SMR CODES	
AFA-035	AEL	PA	FZZ
AH81727	AH	PA	OZZ
A-09226	54495	PA	OZZ
A-10047	OMNI	PA	OZA
A-10125	54495	PA	OZZ
A-11224	54495	PA	OZA
A-11225	54495	PA	OZZ
A-11227	54495	PA	OZZ
A-11238	54495	PA	OZZ
A-11242	54495	PA	OZZ
A-11244	54495	PA	OZZ
A75S-3DB	54495	PA	OZZ
BB1015	01121	PA	FZZ
BB1045	01121	PA	FZZ
BB1265	01121	PA	FZZ
BB1515	01121	PA	FZZ
BB1815	01121	PA	FZZ
BB2205	01121	PA	FZZ
BB2245	01121	PA	FZZ
BB2205	01121	PA	FZZ
BB3305	01121	PA	FZZ
BB3315	01121	PA	FZZ
BB3905	01121	PA	FZZ
BB47S5	01121	PA	FZZ
BB4705	01121	PA	FZZ
BB5105	01121	PA	FZZ
BB6215	01121	PA	FZZ
BB7505	01121	PA	FZZ
BB8205	01121	PA	FZZ
BB8215	01121	PA	FZZ
B-09371	54495	PA	FZZ
B-10830	54495	PA	OZH
B-10831	54495	PA	OZH

PART NUMBER	FSCM	SMR CODES	
B-10834	54495	PA	OZH
B-10835	54495	PA	OZH
B-10837	54495	PA	OZH
B-10838	54495	PA	OZH
B-10839	54495	PA	OZH
B-10844	54495	PA	OZH
B-10852	54495	PA	OZH
B-10856	54495	PA	OZH
B-11024	54495	PA	OZH
B-11026	54495	PA	OZH
B-11027	54495	PA	OZH
B-11029	54495	PA	OZH
B-11051	54495	PA	OZH
B-11052	54495	PA	OZH
B-11256	54495	PA	OZZ
B58535	83594	PA	OZZ
CA-3049	99089	PA	FZZ
CAL-MC-250	CAL	PA	FZZ
CB1005	01121	PA	FZZ
CB1015	01121	PA	FZZ
CB1025	01121	PA	FZZ
CB1045	01121	PA	FZZ
CB1215	01121	PA	FZZ
CB1225	01121	PA	FZZ
CB1235	01121	PA	FZZ
CB1305	01121	PA	FZZ
CB1315	01121	PA	FZZ
CB1515	01121	PA	FZZ
CB1525	01121	PA	FZZ
CB1535	01121	PA	FZZ
CB1545	01121	PA	FZZ
CB1805	01121	PA	FZZ
CB1815	01121	PA	FZZ

NUMERICAL INDEX

PART NUMBER	FSCM	SMR CODES	
CB1825	01121	PA	FZZ
CB1835	01121	PA	FZZ
CB22S5	01121	PA	FZZ
CB2205	01121	PA	FZZ
CB2215	01121	PA	FZZ
CB2235	01121	PA	FZZ
CB2705	01121	PA	FZZ
CB2725	01121	PA	FZZ
CB2735	01121	PA	FZZ
CB3305	01121	PA	FZZ
CB3315	01121	PA	FZZ
CB3325	01121	PA	FZZ
CB3335	01121	PA	FZZ
CB3925	01121	PA	FZZ
CB3935	01121	PA	FZZ
CB3945	01121	PA	FZZ
CB47G5	01121	PA	FZZ
CB47S5	01121	PA	FZZ
CB4115	01121	PA	FZZ
CB4725	01121	PA	FZZ
CB4735	01121	PA	FZZ
CB5105	01121	PA	FZZ
CB5115	01121	PA	FZZ
CB5125	01121	PA	FZZ
CB5605	01121	PA	FZZ
CB5615	01121	PA	FZZ
CB5625	01121	PA	FZZ
CB6215	01121	PA	FZZ
CB6305	01121	PA	FZZ
CB6815	01121	PA	FZZ
CB6825	01121	PA	FZZ
CB7505	01121	PA	FZZ
CB7515	01121	PA	FZZ

PART NUMBER	FSCM	SMR CODES	
CB8205	01121	PA	FZZ
CB8215	01121	PA	FZZ
CB8235	01121	PA	FZZ
CB9115	01121	PA	FZZ
C-09432	54495	PA	OZH
C-10769	54495	PA	OZH
C-10770	54495	PA	OZH
C-11145	54495	PA	OZZ
C280AE/P100K	28092	PA	FZZ
DD-102	71590	PA	FZZ
DD-203	71590	PA	FZZ
D-09367	54495	PA	FZZ
D-10768	54495	PA	FZZ
D-11264	54495	PA	FZZ
D155F020J0	53021	PA	FZZ
D155F050J0	53021	PA	FZZ
D155F080J0	53021	PA	FZZ
D155F100J0	53021	PA	FZZ
D155F110J0	53021	PA	FZZ
D155F115J0	53021	PA	FZZ
D155F151J0	53021	PA	FZZ
D155F152J0	53021	PA	FZZ
D155F220J0	53021	PA	FZZ
D155F221J0	53021	PA	FZZ
D155F230J0	53021	PA	FZZ
D155F331J0	53021	PA	FZZ
D155F470J0	53021	PA	FZZ
D0-218-B	21847	PA	FZZ
EB2215	01121	PA	FZZ
FDH666	13715	PA	FZZ
FTIH000	71590	PA	FZZ
GB47S5	01121	PA	FZZ
GB5605	01121	PA	FZZ

NUMERICAL INDEX

PART NUMBER	FSCM	SMR CODES	
GPD402	ANA	PA	FZZ
HPA2800	28480	PA	FZZ
LM307N	83781	PA	FZZ
LM309-K	83781	PA	FZZ
LM320-K-5.2	83781	PA	FZZ
LM320-K-12	83781	PA	FZZ
LM320-K-18	83781	PA	FZZ
LM741N	83781	PA	FZZ
MC10124	04713	PA	FZZ
MC10131	04713	PA	FZZ
MC10231	04713	PA	FZZ
MC1039P	04713	PA	FZZ
MC1661	04713	PA	FZZ
MC1663	04713	PA	FZZ
MC3008	04713	PA	FZZ
MC3062	04713	PA	FZZ
MC4040	04713	PA	FZZ
MC836P	04713	PA	FZZ
MC846	04713	PA	FZZ
MC909H	04713	PA	FZZ
MJE6044	04713	PA	FZZ
MMT3960	04713	PA	FZZ
MMT8015	04713	PA	FZZ
MP1181	04713	PA	FZZ
MV2107	04714	PA	FZZ
MZ92-109B	04713	PA	FZZ
RODAN 8FK5	54495	PA	FZZ
RMC-Z5U	56289	PA	FZZ
RN55D1001F	01121	PA	FZZ
RN55D1022F	01121	PA	FZZ
RN55D1213F	01121	PA	FZZ
RN55D2001F	01121	PA	FZZ
RN55D2210F	01121	PA	FZZ

PART NUMBER	FSCM	SMR CODES	
RN55D3093F	01121	PA	FZZ
RN55D3740F	01121	PA	FZZ
RN55D4873F	01121	PA	FZZ
RN55K4992F	01121	PA	FZZ
RN55D6001F	01121	PA	FZZ
RN55D8061F	01121	PA	FZZ
RN55K8445F	01121	PA	FZZ
SB-3796A	71450	PA	FZZ
SCO4BN102AK	14099	PA	FZZ
SC21BY330K	WEST	PA	FZZ
SC22904L	WEST	PA	FZZ
SC26BY150	14099	PA	FZZ
SK-207	83594	PA	FZZ
SN4141	01295	PA	FZZ
SN74L86	01295	PA	FZZ
SN74LS73	01295	PA	FZZ
SN7400	01295	PA	FZZ
SN7401	01295	PA	FZZ
SN7402	01295	PA	FZZ
SN7404	01295	PA	FZZ
SN7405	01295	PA	FZZ
SN7410	01295	PA	FZZ
SN74121	01295	PA	FZZ
SN74196	01295	PA	FZZ
SN7440	01295	PA	FZZ
SN7442	01295	PA	FZZ
SN7451	01295	PA	FZZ
SN7473	01295	PA	FZZ
SN7490	01295	PA	FZZ
SN7493	01295	PA	FZZ
SN8280	01295	PA	FZZ
TG-D50	01884	PA	FZZ
TG-S10	01884	PA	FZZ

NUMERICAL INDEX

PART NUMBER	FSCM	SMR CODES	
TXB2P-032-037	IERC	PA	FZZ
T-206 Series	71450	PA	FZZ
UG-1094	02660	PA	FZZ
V53-1 Series	18612	PA	FZZ
000211	54495	PA	FZZ
004231	54495	PA	FZZ
004586	54495	PA	FZZ
005136	54495	PA	FZZ
006245	54495	PA	FZZ
006792	54495	PA	FZZ
1N3605	04713	PA	FZZ
1N4005	07263	PA	FZZ
1N4576	07263	PA	FZZ
1N4997	07263	PA	FZZ
1N695	07263	PA	FZZ
1N749A	07263	PA	FZZ
1N751A	04713	PA	FZZ
1N753A	07263	PA	FZZ
1N756A	04713	PA	FZZ
1N914	07263	PA	FZZ
1025-08	99800	PA	FZZ
1025-10	99800	PA	FZZ
1025-16	99800	PA	FZZ
1025-20	99800	PA	FZZ
1025-28	99800	PA	FZZ
15D2224X002	53021	PA	FZZ
191TE1A1-55	53021	PA	FZZ
198D	53021	PA	FZZ
2N3400	07263	PA	FZZ
2N3440	07263	PA	FZZ
2N3563	07263	PA	FZZ
2N3565	04713	PA	FZZ
2N3640	07263	PA	FZZ

PART NUMBER	FSCM	SMR CODES	
2N3646	04713	PA	FZZ
2N4123	07263	PA	FZZ
2N4124	04713	PA	FZZ
2N4126	04713	PA	FZZ
2N4425	07263	PA	FZZ
2N5179	07263	PA	FZZ
2N5400	07263	PA	FZZ
2N5833	04713	PA	FZZ
2N6255	07263	PA	FZZ
2020-5100	AMI	PA	FZZ
2087-1220	AMI	PA	FZZ
23C25TS33	53021	PA	FZZ
3009P	51641	PA	FZZ
313.002	75915	PA	OZZ
32-10715	54495	PA	FZF
32-10723	54495	PA	OHF
32-10724	54495	PA	OHF
32-10726	54495	PA	OHF
32-10727	54495	PA	OHF
32-10729	54495	PA	OHF
32-10730	54495	PA	OHF
32-10731	54495	PA	OHF
32-10865	54495	PA	OHF
33-09446	54495	PA	ZHF
33-09449	54495	PA	ZHF
33-09622	54495	PA	ZHF
33-09719	54495	PA	ZHF
33-09720	54495	PA	OHF
33-09723	54495	PA	ZHF
34-09571	54495	PA	ZHF
34-09572	54495	PA	ZHF
34-09609	54495	PA	ZHF
34-09610	54495	PA	ZHF

NUMERICAL INDEX

PART NUMBER	FSCM	SMR CODES	
34-09715	54495	PA	ZHF
34-09720	54495	PA	ZHF
34-09733	54495	PA	ZHF
34-09734	54495	PA	ZHF
34-11225	54495	PA	ZHF
43014	75915	PA	FZZ
46206LFR	SWT	PA	FZZ
46256LFR	SWT	PA	FZZ
50PK2	18677	PA	FZZ
500-1918-01	72982	PA	FZZ
50-09137	54495	PA	FZZ
50-09178	54495	PA	FZZ
50-09429	54495	PA	FZZ
50-09434	54495	PA	FZZ
50-448-10	18677	PA	FZZ
51-043-0000	98291	PA	FZZ
51-047-0000	98291	PA	FZZ
51-051-0000	98291	PA	FZZ
538-002-94R-3-5	72282	PA	FZZ
538-002-94R-7-35	72282	PA	FZZ
538-011-NOP-2-8	72282	PA	FZZ
62P	51641	PA	FZZ
672P-3-P	05820	PA	FZZ
70-09139	54495	PA	FZZ
79PR1K	05721	PA	FZZ
79PR102	05721	PA	FZZ
79PR503	05721	PA	FZZ
79-10282	54495	PA	LLD
79-10499	54495	PA	LLD
79-10599	54495	PA	LLD
79-10836	54495	PA	LLD
811-25V-103P	54495	PA	FZZ
95-09188	54495	PA	FZZ

AUTO HET ASSEMBLY (A1)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1	Auto Het Assy	EI	34-10715		REF
A1	Input Amplifier and Prescaller PCB Assy	EI	32-10731		1
A2	Input Control and 1st DCU PCB Assy	EI	32-10865		1
A3	Sweep Generator PCB Assy	EI	32-10729		1
A4	Start Detector and Preset "N" Counter PCB Assy	EI	32-10728		1
A5	D/A Converter PCB Assy	EI	32-10727		1
A6	YIG Driver and Controller PCB Assy	EI	32-10726		1
A7	Stop Detector and IF Shaper PCB Assy	EI	32-10724		1
A8	YIG Tuned Multiplier Assy	OMNI	A-10047	006785	1
A9	200 MHz Power Amplifier Assy	EI	34-09571		1
A10	Low Pass Filter Assy	EI	A-10125	006784	1
A12	200 MHz Frequency Multiplier Assy	EI	34-09572		1
A13	IF Amplifier Assy	EI	34-10734		1
A14	Hybrid Coupler Assy	AMI	2020-5100		1
A15	Back Diode Detector Assy	AER	D0-218-B		1
A16	Auto Het Mother Board PCB Assy	EI	33-10723		1
A17	Attenuator Assy	AEL	AFA-035	007135	1
CR1	Diode, Signal, 1N4005	MOT	1N4005	003663	1
J1, 2	Connector, Adapter Coax SMA Right Angle	AMI	2087-1220	007135	2
MP1	Chassis, RF	EI	D-11264	007159	1
MP2	Bracket, Mounting, Potentiometer	EI	B-11265	007160	1
Q1, 2	Transistor, Power Type MJE 6044	MOT	MJE 6044	007158	2
R1	Resistor, Power, with Heat Sink, 4 Ω, 25W, 1%	CAL	CAL-MC-250	005294	1
R2	Potentiometer, 50 Ω	EI		006759	1

INPUT AMPLIFIER AND PRESCALER PCB ASSEMBLY (A1A1) PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A1	Input Amplifier and Prescaler PCB Assy	EI	32-10731	32-10731	REF
C1	Capacitor, 100μF, 4 WVDC	SPR	198D series	006864	1
C2, 25, 30	Capacitor, .001μF, 100 WVDC	CRL	DD-120	000117	3
C3, 7, 8	Capacitor, 39pF, Mica	EI	006245	006245	3
C4, 5, 6, thru 15, 18	Capacitor, .01μF, 100 WVDC	SPR	TG-S10	006158	10
C16, 18	Capacitor .1μF, 250 WVDC, Mylar	AMPE	C280AE/P100K	000211	2
C17, 28	Capacitor 2.2μF, 15 WVDC	STM	198D series	004545	2
C26	Capacitor, .01μF, Chip				1
C27	Capacitor, 200pF				1
C29, 31	Capacitor, 4.7pF				1
CR1, 2, 3	Diode, FDH 666			004471	
CR4, 5	Diode, HPA-2800	HPA	HPA-2800	003067	
E1	P.C. Board	EI	79-10547	006861	1
J1, 2, 3, 4	Connector Coax, SMA	SEAL	51-051-0000	000432	4
K1	Relay, Reed	SIGM	191TE1A1-55	006856	1
Q1, 2	Transistors, Matched pair FET	EI	27-10362	006863	1 pr
Q3	Transistor MPS H81	MOT	MPS H81	006863	1
Q4	Transistor 2N4124	MOT	2N4124	003294	1
Q5, 6	Transistor, MMT 8015 Small Signal RF	MOT	MMT8015		2
Q9 thru Q25	Transistor MMT 3960	MOT	MMT3960	006898	18
R1	Resistor, C.C., 56Ω, 1W, 5%	AB	GB5605	001269	1
R3, 5, 13	Resistor, C.C. 820Ω, 1/8W, 5%	AB	BB8215	001053	2
R4	Potentiometer, 200Ω	BRNS	62P	000934	1
R6, 17, 18, 19 34, 35, 54	Resistor, C.C., 510Ω	AB	BB5115	003136	7
R7	Resistor, C.C. 1.2M, 1/8W, 5%	AB	BB1265	003138	1
R8	Resistor, C.C. 100K, 1/8W, 5%	AB	BB1045	001061	1

INPUT AMPLIFIER AND PRESCALER
PCB ASSEMBLY (A1A1)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R9	Resistor C.C. 4.7Ω 1/8W, 5%	AB	BB47S5	001058	1
R10, 11, 12	Resistor C.C., 39Ω 1/8W, 5%	AB	BB3905	001070	4
R14	Resistor C.C., 47Ω 1/8W, 5%	AB	BB4705	001041	1
R15, 39, 40, 57	Resistor C.C., 150Ω 1/8W, 5%	AB	BB1515	001046	4
R16, 43	Resistor C.C., 330Ω 1/8W, 5%	AB	BB3315	001050	2
R20	Resistor, C.C. 18Ω, 1/4W, 5%	AB	CB1805	001070	1
R21	Resistor, C.C. 510Ω 1/4W, 5%	AB	CB5115	001093	1
R22	Resistor C.C., 680Ω 1/4W, 5%	AB	CB6815	001096	1
R23	Resistor, C.C., 180Ω 1/4W, 5%	AB	CB1815	001084	1
R25, 28, 29, 44	Resistor, C.C., 240Ω 1/8W, 5%	AB	BB2415		4
R26	Resistor, C.C., 51Ω 1/8W, 5%	AB	BB5105	001042	1
R30 thru 33	Resistor, C.C., 22Ω 1/8W, 5%	AB	BB2205	001037	4
R36	Resistor, C.C., 33Ω 1/8W, 5%	AB	BB3305	001039	1
R37, 45	Resistor, C.C. 75Ω 1/4W, 5%	AB	CB7505	003174	2
R38	Resistor, C.C., 82Ω 1/8W, 5%	AB	BB8205	003133	1
R46	Resistor, C.C. 27Ω 1/8W, 5%	AB	BB2705	001038	1
R47	Resistor, C.C., 27Ω 1/4W, 5%	AB	CB2705	001072	1

INPUT AMPLIFIER AND PRESCALER
PCB ASSEMBLY (A1A1)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R48	Resistor, C.C., 180Ω 1/8W, 5%	AB	BB1815	001047	1
R49	Resistor, C.C., 620Ω 1/8W, 5%	AB	BB6215	001053	1
R50	Resistor, C.C., 4.7K 1/8W, 5%	AB	BB4725	001058	1
R52, 53	Resistor, C.C., 100Ω 1/8W, 5%	AB	BB1015	001044	2
U1	Intergrated Circuit Type SC22904L		SC22904L		1

INPUT CONTROL AND 1ST DCU
PCB ASSEMBLY (A1A2)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A2	Input Control and 1st DCU PCB Assy	EI	32-10865	32-10865	REF
C1, 4 thru 14	Capacitor, .01μF, 100 WVDC	SPR	TG-S10	000158	10
C2, 3, 17, 18	Capacitor, .1μF, 250 WVDC	AMPE	C280AE/P100K	000211	4
C19, 20	Capacitor, 2.2μF, 15 WVDC	STM	198D series	004545	2
E1	P. C. Board	EI	79-10836	006856	1
J1 thru 4	Connector, coax SMA	SEAL	51-051-0000	000432	4
Q1 thru 4	Transistor, 2N3563	MOT	2N3563	003262	4
R1, 4, 9, 32	Resistor, C.C., 82Ω 1/4W, 5%	AB	CB8205	001080	4
R2, 20	Resistor, C.C., 2.2K 1/4W, 5%	AB	CB2225	001103	2
R3, 14, 17, 18, 36	Resistor, C.C. 820Ω 1/4W, 5%	AB	CB8215	001097	5
R5, 6, 24 thru 28	Resistor, C.C. 130Ω 1/4W, 5%	AB	CB1315	003176	10
R7, 8, 30, 31, 33, 34, 35, 37	Resistor, C.C., 510Ω 1/4W, 5%	AB	CB5115	001093	8
R10, 11, 13 41	Resistor, C.C., 680Ω 1/4W, 5%	AB	CB6815	001096	4
R12	Resistor, C.C. 560Ω 1/4W, 5%	AB	CB5615	001094	1
R15, 16	Resistor, C.C., 750Ω 1/4W, 5%	AB	CB7515	003179	2
R19, 45	Resistor, C.C., 1K 1/4W, 5%	AB	CB1025	001098	2
R21, 22, 23	Resistor, C.C., 390Ω 1/4W, 5%	AB	CB3915	001091	3
R38, 39, 40 41, 42	Resistor, C.C., 180Ω 1/4W, 5%	AB	CB1815	001084	5

INPUT CONTROL AND 1ST DCU
PCB ASSEMBLY (A1A2)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R44	Resistor, C.C., 330Ω 1/4W, 5%	AB	CB3315	001090	1
U1	Intergrated Circuit Type MC 10124	MOT	MC 10124	006858	1
U2	Intergrated Circuit Type MC 1663	MOT	MC 1663		1
U3	Intergrated Circuit Type MC 1161	MOT	MC 1661	005279	1
U4	Intergrated Circuit Type MC 10131	MOT	MC 10131	005282	1
U5	Intergrated Circuit Type MC 10231	MOT	MC 10231	006859	1
U6	Intergrated Circuit Type MC 1039P	MOT	MC 1039P	005278	1

SWEEP GENERATOR PCB ASSEMBLY (A1A3) PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A3	Sweep Generator PCB Assy	EI	32-10729	32-10729	REF
C1, 3, 4, 9, 10, 11	Capacitor, .01μF, Cer, Disk., 100 WVDC	SPR	TG-S10	000158	6
C2	Capacitor, 0.1μF, Mylar			000211	1
C5	Capacitor, .001μF, Cer., 250 WVDC	AMPE	C280AE/P100K	000116	1
C7, 8	Capacitor, 1000 pF			000003	2
CR1	Diode, FDH666	FAI	FDH666	004471	1
E1	P. C. Board	EI	79-10281	006736	1
J1, 2	Socket, IC DIP 14 pin	EI		005136	2
Q1, 2	Transistor, 2N3646	MOT	2N3646	001731	2
Q3	Transistor, 2N3565	MOT	2N3565	003436	1
R1	Resistor, C.C., 4.7Ω 1/4W, 5%	AB	CB47S5	001066	1
R2, 3, 6	Resistor, C.C., 2.7K, 1/4W, 5%	AB	CB2725	001103	3
R4, 5, 7, 13, 14, 15	Resistor, C.C., 3.3K, 1/4W, 5%	AB	CB3325	001107	6
R8	Resistor, C.C., 2.2K, 1/4W, 5%	AB	CB2225	001103	1
R9, 10	Resistor, C.C., 18K, 1/4W, 5%	AB	CB1835	001119	2
R11, 12	Resistor, C.C., 4.7K, 1/4W, 5%	AB	CB4725	001109	2
R17 thru 25	Resistor, C.C., 1.2K, 1/4W, 5%	AB	CB1225	001099	9
U1	Intergrated Circuit, Type 7404	TI	SN7404	004518	1
U2, 5	Intergrated Circuit, Type 7402	TI	SN7402	004516	2
U3	Intergrated Circuit, Type 7410	TI	SN7410	004520	1
U4, 6, 8	Intergrated Circuit, Type 7486	TI	SN74L86	005289	3

SWEEP GENERATOR PCB
ASSEMBLY (A1A3)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
U7, 9	Intergrated Circuit, Type 7405	TI	SN7405	004519	2
U10, 12, 14	Intergrated Circuit, Type 74196	TI	SN74196	004699	3
U11, 13	Intergrated Circuit, Type 7490	TI	SN7490	004729	2

START DETECTOR AND "N" PRESET COUNTER PCB ASSEMBLY (A1A4) PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A4	Start Detector and "N" Preset Counter PCB Assy	EI	32-10728	32-10728	REF
C1, 2	Capacitor, 1μF, Tant	SAN		004586	2
C3, 4	Capacitor, .01μF, 100 WVDC, Cer.	SPR	TG-S10	000158	2
C5	Capacitor, .1μF, 250 WVDC Mylar	AMPE	C280AE/P100K	000211	1
CR1	Diode, 1N749A	MOT	1N749A	000527	1
E1	P. C. Board	EI	79-10329	006735	1
Q1, 2	Transistor 2N3646	MOT	2N3646	001731	1
R1	Resistor, C.C., 51Ω 1/4W, 5%	AB	CB5105	001076	1
R3, 9	Resistor, C.C., 2.7K 1/4W, 5%	AB	CB2725	001105	2
R4, 8	Resistor, C.C., 8.2K 1/4W, 5%	AB	CB8225	001115	2
R5	Potentiometer, 5K	BECK	79P R503	000988	1
R6, 12	Resistor, C.C., 3.3K 1/4W, 5%	AB	CB3325	001107	2
R7	Resistor, C.C., 1K 1/4W, 5%	AB	CB1025	001098	1
R10	Potentiometer, 10K	BECK	79P R103	004511	1
R11	Resistor, C.C., 470K 1/4W, 5%	AB	CB4745	001141	1
R14, 15	Resistor, C.C., 4.7K 1/4W, 5%	AB	CB4725	001066	2
U1	Intergrated Circuit, Type 7410	TI	SN7410	004520	1
U2, 3, 4	Intergrated Circuit, Type 7490	TI	SN7490	004729	3
U5	Intergrated Circuit, Type 7404	TI	SN7404	004518	1
U6, 7, 8	Intergrated Circuit, Type 7486	TI	SN74L86	005289	3

START DETECTOR AND "N" PRESET
COUNTER PCB ASSEMBLY (A1A4)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty
U9, 10	Intergrated Circuit	TI	SN7405	004519	2
U11	Intergrated Circuit Operational Amplifier	NAT	LM301AN		1
U12	Intergrated Circuit Operational Amplifier	NAT	LM741N		1

D/A CONVERTER PCB ASSEMBLY (A1A5)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A5	D/A Converter PCB Assy	EI	32-10727	32-10727	REF
C1	Capacitor, 1μF, Tant	SAN		004586	1
C2, 8	Capacitor, .01μF, Cer.	SPR	TG-S10	000158	2
C3 thru 7	Capacitor, .1μF, 250 WVDC, Mylar	AMPE	C280AE/P100K	000211	5
CR1	Diode, 1N4576	MOT	1N4576	004257	1
E1	P. C. Board	EI	79-10282	006737	1
Q1 thru 14 16 thru 20	Transistor, 2N4126	MOT	2N4126	003267	19
Q15	Transistor, 2N4124	MOT	2N4124	003294	1
R1, 5, 9 13	Resistor, Metal Film, 10.2K, 1%	AB	RNR55D1022F	006739	4
R2, 17, 52	Resistor, Metal Film, 487K, 1%	AB	RNR55D4873F	005321	3
R3, 7, 11, 19, 37, 53, 57, 61, 65,	Resistor, Metal Film, 1.13K, 1%	AB	RNR55D1131F	006739	9
R4, 8, 12, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34	Resistor, C.C. 2.2K 1/4W, 5%	AB	CB2225	001103	13
R10, 21, 60	Resistor, Metal Film, 121K, 1%	AB	RNR551213F	005323	3
R14, 23, 64	Resistor, Metal Film, 60K, 1%	AB	RNR556001F	005324	3
R25, 45	Resistor, Metal Film, 48K, .3W, .02%	VIS	V53-1 series	005302	2
R27, 47	Resistor, Metal Film, 24K, .3W, .02%	VIS	V53-1 series	005295	2
R29	Resistor, Metal Film, 12K, .3W, .02%	VIS	V53-1 series	005296	1
R31, 41	Resistor, Metal Film, 6K, .3W, .02%	VIS	V53-1 series	005307	2

D/A CONVERTER PCB ASSEMBLY (A1A5)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R33	Resistor, Metal Film, 4.8K, .3W, .02%	VIS	V53-1 series	005308	1
R35	Resistor, Metal Film 2.4K, .3W, .02%	VIS	V53-1 series	005309	1
R38	Potentiometer, 50K	BECK	79P R503	004412	1
R42	Potentiometer, 1K	BECK	79P R102	004410	1
R48	Resistor, C.C., 750K 1/4W, 5%	AB	CB7535	006738	1
R49	Resistor, C.C., 1K 1/4W, 5%	AB	CB1025	001098	1
R51, 55, 59, 63	Resistor, Metal Film	VIS	V53-1 series	006746	4
R67, 68, 80	Resistor, C.C., 4.7K 1/4W, 5%	AB	CB4725	001066	3
U1, 2, 3	Intergrated Circuit, Type MC 837P	MOT	MC 837P	003614	3
U4, 5	Intergrated Circuit, Type MC LM 307N	NAT	LM 307N	005291	2

YIG DRIVER AND CONTROLLER PCB ASSEMBLY (A1A6) PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A6	YIG Driver and Controller PCB Assy	EI	32-11211		REF
C2, 3, 5, 7, 9	Capacitor, .1μF, 250 WVDC	AMPE	C28AE/P100K	000211	5
C4, 6	Capacitor, 22μF, 15 WVDC	SPR	198D series	004545	2
C8	Capacitor, 33pF	SAN	D155F330J0	000059	1
CR1	Diode, Signal, 1N914	FAI	1N914	004455	1
Q1	Transistor, 2N4126	MOT	2N4126	003267	1
R3	Resistor, C.C., 12K, 1/4W, 5%	AB	CB1235	001117	1
R4	Resistor, Metel Film, 24K, .3W, .02%	VIS	V53-1	005295	1
R7	Resistor, Metal Film, 237K, .1W, 1%	SPR	RN55D2373F	005297	1
R11	Resistor, Metal Film, 8.06K, .1W, 1%	SPR	RN55D8061F	005300	1
R12, 15	Resistor, C.C., 4.7Ω, 1/4W, 5%	AB	CB47S5	001066	2
R13	Potentiometer, 1K	BECK	79PR1K	004410	1
R14, 16	Resistor, C.C., 4.7K, 1/4W, 5%	AB	CB4735	001109	2
R17	Resistor, C.C., 18K, 1/4W, 5%	AB	CB1835	000119	1
R18	Resistor, C.C., 2.7K, 1/4W, 5%	AB	CB2725	005028	1
R19	Resistor, Metal Film, 12K, .3W, .02%	VIS	V53-1	005296	1
U1	Intergrated Circuit, Operational Amplifier	NAT	LM301AN	005318	1
VR1, 2	Diode, Zener, 1N753A	FAI	1N753A	000531	2

STOP DETECTOR AND IF SHAPER
PCB ASSEMBLY (A1A7)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A7	Stop Detector and IF Shaper PCB Assy	EI	32-10724	32-10724	REF
C1, 36	Capacitor, .001μF, Ceramic	CRL	DD203	000117	2
C2 thru 10, 17 thru 22, 26 thru 29, 31, thru 35	Capacitor, .01μF, 100 WVDC, Ceramic	SPR	TG-S10	000158	23
C12, 14	Capacitor, 8pF, Mica disk	SPR	D155F080J0	000032	2
C15, 16	Capacitor, 330 pF, Mica disk	SPR	D155F331J0	000095	2
C23	Capacitor, 1μF, 35 WVDC			004231	1
C24, 34	Capacitor, .1μF, 250 WVDC Mylar	AMPE	C280AE/P100K	000211	2
C25	Capacitor, Variable, 9-35pF	EER	538-002-94R-9-35	000340	1
C30	Capacitor, 1μF, 35 WVDC			004586	1
CR3	Diode, Zener, 1N756A	COML	1N756A	000534	1
CR5, 6, 7, 8	Diode, HPA2800	HPA	HPA2800	003067	4
CR9	Diode, Zener, 1N751A	MOT	1N751A	000529	1
CR10, 11	Diode, 1N3605	MOT	1N3605	000534	1
E1	P. C. Board	EI	C-10382	006834	1
J1, 2	Connector, Coax,	SEAL	51-051-0000	000432	2
L3, 4	Inductor, 75μH	EI	A-11224	007131	2
L5	Inductor, 1.5μH			000659	1
Q1, 3, 4, 8	Transistor, 2N5179	FAI	2N5179	006750	4
Q5, 6, 7	Transistor, 2N3646	FAI	2N3646	001731	3
R1	Resistor, C.C., 56Ω 1/4W, 5%	AB	CB5605	001077	1
R2	Resistor, C.C., 1.5K, 1/4W, 5%	AB	CB1525	001100	1
R3, 71	Resistor, C.C., 150Ω 1/4W, 5%	AB	CB1515	001081	2
R4, 66	Resistor, C.C., 100Ω 1/4W, 5%	AB	CB1015	001081	2

STOP DETECTOR AND IF SHAPER
PCB ASSEMBLY (A1A7)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R5, 7, 12, 15, 63, 72	Resistor, C.C., 2.2K, 1/4W, 5%	AB	CB2225	001103	6
R6, 11, 41, 64	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	4
R9, 10, 16, 17	Resistor, C.C., 51Ω, 1/4W, 5%	AB	CB5105	001076	4
R13, 32	Resistor, C.C., 470Ω, 1/4W, 5%	AB	CB4715	001092	2
R14, 31	Resistor, C.C., 680Ω, 1/4W, 5%	AB	CB6815	001096	2
R19	Resistor, C.C., 130Ω, 1/4W, 5%	AB	CB1315	003176	1
R20	Potentiometer, 5K	BECK	79P R5K	004410	1
R26, 68, 69	Resistor, C.C., 4.7Ω, 1/4W, 5%	AB	CB47S5	001066	3
R27	Resistor, C.C., 75Ω, 1/4W, 5%	AB	CB7505	003174	1
R29	Resistor, C.C., 910Ω, 1/4W, 5%	AB	CB9115	003180	1
R33	Resistor, Metal Film, 374Ω, 1%	SPR	RNR553740F	006836	1
R34, 47, 41	Resistor, Metal Film, 1K, 1%	SPR	RNR551001F	006837	3
R35, 40	Potentiometer, 10K	BRNS	3009P	004551	2
R36	Resistor, Metal Film, 49.9K, 1%	SPR	RNR554992F	006840	2
R37	Resistor, Metal Film, 200K, 1%	SPR	RNR552001F		1
R38	Resistor, Metal Film, 8.45K, 1%	SPR	RNR558451F		1
R39, 62	Resistor, C.C., 10K, 1/4W, 5%	AB	CB1035	001116	2

STOP DETECTOR AND IF SHAPER
PCB ASSEMBLY (A1A7)
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R42, 43, 44, 45	Resistor, Metal Film, 178K	SPR	RNR551783F	006841	4
R46	Resistor, C.C., 390Ω, 1/4W, 5%	AB	CB3905	001091	1
R48	Resistor, Metal Film, 22.1Ω, 1%	SPR	RNR552210F	006835	1
R49	Resistor, Metal Film, 3.09K, 1%	SPR	RNR553093F	006838	1
R50	Potentiometer, 100Ω			004408	
R51	Resistor, C.C., 100K, 1/4W, 5%	AB	CB1045	001131	1
R52, 54	Resistor, C.C., 5.6K, 1/4W, 5%	AB	CB5625	001111	2
R53, 60, 65	Resistor, C.C., 3.3K, 1/4W, 5%	AB	CB6325	001107	3
R55	Resistor, C.C., 6.8K, 1/4W, 5%	AB	CB6825	001113	1
R68	Resistor, C.C., 4.7K, 1/4W, 5%	AB	CB4725	001109	1
U1, 2	Intergrated Circuit, Type 7400	TI	SN7400	004302	2
U3	Intergrated Circuit, Type 846	MOT	MC846	003621	1
U4, 5, 6	Intergrated Circuit, Type LM741N	NAT	LM741N	006354	3
U7	Intergrated Circuit Type CA-3049	RCA	CA-3049		1

STOP DETECTOR AND IF SHAPER
PCB ASSEMBLY (A1A7)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
A1A7	Stop Detector and IF Shaper PCB Assy.	EI	32-10724		REF
C1, 10-21, 24, 28-32, 34, 37, 39, 40	Capacitor, Ceramic .01μF, 100 WVDC	SPR	TG-S10	000158	23
C2, 22, 23	Capacitor, Mica 330 pF	SAN	D155F331JO	000095	3
C3, 5	Capacitor, Mica 18 pF	SAN	D155F180JO	000042	2
C4, 7	Capacitor, 22μF, 15 WVDC	SPR	196D226X9015KA1	004645	2
C6, 8	Capacitor, Ceramic .001μF	CRL	DD203	000117	2
C9	Capacitor, Mica 180 pF	SAN	D155F181JO	000067	1
C25, 27	Capacitor, Mica 8 pF	SAN	D155F080JO	000032	2
C26	Capacitor, Variable 9-35 pF	EER	538-002-94R-9-35	000340	1
C33, 36	Capacitor, Mylar .1μF 35 WVDC	AMPE	C280AE/P100K	000211	2
C35	Capacitor, Mylar 6.4μF	AMPE	C426ARF6.4	004231	1
C38	Capacitor, Tant 1μF	SPG	CSR13G105KM	004586	1
CR1, 3-5	Diode	HPA	HPA2800	003067	4
CR2	Diode Zener	MOT	1N756A	000534	1
CR6	Diode Zener	MOT	1N751A	000529	1
CR7, 8	Diode	MOT	1N3605	000550	2
E1	P. C. Board	EI	C-10382		1
J1, 2	Connector Coax	SEAL	51-051-0000	000432	2
L1, 3	Inductor Assy	EI	A-11224		2
L2	Inductor 1.5μH	DEL	1025-24	000659	1
Q1-4	Transistor	FAI	2N5179	006750	4
Q5-7	Transistor	FAI	2N3646	001731	3
R1	Resistor, Variable 5K	BECK	79PR5K	004411	1
R2	Resistor, Variable 100Ω	BRNS	3009P1101	004408	1
R3, 4	Resistor, Variable 10K	BRNS	3009P1103	004551	1
R5	Resistor, C.C. 56Ω 1/4W	AB	CB5605	001077	1

STOP DETECTOR AND IF SHAPER

PCB ASSEMBLY (A1A7)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R6	Resistor, C.C., 4.7K, 1/4W	AB	CB4725	001109	1
R7	Resistor, C.C., 270Ω, 1/4W	AB	CB2715	001088	1
R8, 63	Resistor, C.C., 100Ω, 1/4W	AB	CB1015	001081	2
R9, 14	Resistor, C.C., 150Ω, 1/4W	AB	CB1515	001083	2
R10	Resistor, C.C., 1.5Ω, 1/4W	AB	CB1525	001100	1
R11	Resistor, C.C., 3.9KΩ, 1/4W	AB	CB3925	001108	1
R12, 53	Resistor, C.C., 620Ω, 1/4W	AB	CB6215	001095	2
R13	Resistor, C.C., 47Ω, 1/4W	AB	CB4705	001075	1
R15	Resistor, C.C., 910Ω, 1/4W	AB	CB9115	003180	1
R16	Resistor, C.C., 75Ω, 1/4W	AB	CB7505	003174	1
R17, 19, 21, 23, 25, 61	Resistor, C.C., 2.2KΩ, 1/4W	AB	CB2225	001103	6
R18, 26, 27, 35	Resistor, C.C., 4.7Ω, 1/4W	AB	CB4R75	001066	4
R20, 33, 62	Resistor, C.C., 1KΩ, 1/4W	AB	CB1025	001098	3
R22	Resistor, C.C., 680Ω, 1/4W	AB	CB6815	001096	1
R24, 39	Resistor, C.C., 470Ω, 1/4W	AB	CB4715	001092	2
R28, 40, 47	Resistor, Metal Film, 1KΩ, 1/4W, 1%	AB	RN55D1001	006837	3
R29, 30, 37, 38	Resistor, C.C., 51Ω, 1/4W	AB	CB5105	001076	4
R31, 32	Resistor, C.C., 3.6K, 1/4W	AB	CB3625	005339	2
R34	Resistor, C.C., 130Ω, 1/4W, 5%	AB	CB1315	003176	1
R36, 46, 49, 50	Resistor, Metal Film, 178K, 1/4W, 1%	AB	RN55D1783	006841	4
R41	Resistor, Metal Film, 22.1Ω, 1/4W, 1%	AB	RN55D22R1	006835	1
R42	Resistor, C.C., 100K, 1/4W	AB	CB1045	001131	1
R43	Resistor, Metal Film, 3.09KΩ, 1/4W, 1%	AB	RN55D3091	006838	1

STOP DETECTOR AND IF SHAPER

PCB ASSEMBLY (A1A7)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R44	Resistor, Metal Film, 374Ω, 1/4W, 1%	AB	RN55D3740	006836	1
R45	Resistor, C.C., 390Ω, 1/4W, 5%	AB	CB3915	001091	1
R48	Resistor, Metal Film, 49.9KΩ, 1/4W, 1%	AB	RN55D4992	006840	1
R51, 52	Resistor, C.C., 5.6KΩ, 1/4W, 5%	AB	CB5625	001111	2
R54	Resistor, C.C., 180KΩ, 1/4W, 5%	AB	CB1845	001134	1
R55	Resistor, C.C., 8.2KΩ, 1/4W, 5%	AB	CB8225	001115	1
R56	Resistor, C.C., 330Ω, 1/4W, 5%	AB	CB3315	001090	1
R57, 64-66, 69	Resistor, C.C., 3.6KΩ, 1/4W, 5%	AB	CB3625	001107	5
R58, 59, 67, 70	Resistor, C.C., 10KΩ, 1/4W, 5%	AB	CB1035	001116	4
R60	Resistor, C.C., 560Ω, 1/4W, 5%	AB	CB5615	001094	1
R68	Resistor, C.C., 5.6KΩ, 1/4W, 5%	AB	CB5625	001113	1
U1	Integrated Circuit	RCA	CA3102E		1
U2-4	Integrated Circuit	NAT. SEMI.	LM741N	006354	3
U5	Integrated Circuit	MOT	MC846P	003621	1
U6, 7	Integrated Circuit	MOT	MC7400	004302	2

200 MHZ POWER AMPLIFIER ASSEMBLY (A1A9)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty
A1A9	200 MHZ Power Amplifier Assy.	EI	34-09571	34-09571	REF
A1	Case Assembly	EI	50-09429	049429	1
C1, 2, 3, 4, 9, 12	Capacitor, Variable 7-35pF	EER	538-002-94R-7-35	005097	6
C5, 8, 11, 15	Capacitor, 01μF, 100 WVDC	SPR	TG-S10	000158	4
C10	Capacitor, 10pF, Mica Disk	SAN	D155F100J0	000034	1
C13	Capacitor, 15pF, Mica Disk	SAN	D155F150J0	000038	1
C14	Capacitor, .001μF, 100 WVDC	CLR	DD-120	000117	1
C16	Capacitor, 22μF, 15 WVDC	SPR	198D series	004645	1
C17, 18	Capacitor, 1000pF, Feed-thru	CRL	FT 1000	005263	2
E1	P.C. Board	EE	33-09446	049169	1
E2, 3	Heat Sink	IERC	TXB2P-032-037	000629	2
J1	Connector, Coax, SMA	SOL	2970-6002	000432	1
J2	Connector, Coax	SEA	51-047-0000	000430	1
L1, 5, 9, 10	Inductor, 4 Turns #20 AWG buss wire .25" Dia.	EE	006792	006792	4
L2	Inductor, .33μH	DEL	1025-08	000651	1
L6	Inductor, .68μH	DEL	1025-16	000655	1
L8	Inductor, 1μH	DEL	1025-20	000657	1
Q1	Transistor, 2N6255	FAI	2N6255	006755	1
Q2, 3	Transistor, 2N4425	FAI	2N4425	006754	1
R1	Resistor, C.C., 120Ω, 1/4W, 5%	AB	CB1215	001082	1
R2	Resistor, C.C., 220Ω, 1/4W, 5%	AB	CB2215	001086	1
R3	Resistor, C.C. 51Ω, 1/4W, 5%	AB	CB5105	001076	1
R4	Resistor, C.C. 1.5K, 1/4W, 5%	AB	CB1525	001100	1
R5	Resistor, C.C., 680Ω, 1/4W, 5%	AB	CB6815	001096	1
R7	Resistor, C.C. 4.7Ω, 1/4W, 5%	AB	CB47S5	001066	1
R8	Resistor, C.C., 2.2Ω, 1/4W, 5%	AB	CB22S5		1

200 MHZ FREQUENCY MULTIPLIER ASSEMBLY (A1A11)

PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty
A1A11	200 MHz Freq. Mult. Assy.	EI	33-09449		REF
C1	Capacitor, .001μF, 100 WVDC	CRL	DD-120	000117	1
C2, 3, 7, 9, 13, 19	Capacitor, Variable, 9-35pF	EER	538-002-94-R-9-35	000340	6
C4, 5, 11, 14, 16, 17	Capacitor, .001μF, Chip	SEMT	SC04BN102AK	003010	6
C6, 8	Capacitor, 2pF, Mica Disk, 500 WVDC	SAN	D155F020J1	000026	2
C10, 15, 18	Capacitor, fpF, Mica Disk, 500 WVDC	SAN	D155F050J1	000028	3
C12	Capacitor, 10pF, Mica Disk, 500 WVDC	SAN	D155F110J0	003005	1
C18	Capacitor, 15pF, Mica Disk, 500 WVDC	SAN	D155F115J0	000038	1
C20	Capacitor, .01uFd, 100 WVDC	SPR	TG-S10	000158	1
C21	Capacitor, 1000pF, Feed-thru	CRL	FT 1000	005263	1
E1	P.C. Board	EI	33-09449	049170	1
E2	Case, Assembly	EI		049420	1
J1, 2	Connector, Coax	SEAL	51-047-0000	000430	2
L1	Inductor, 2.2μH	DEL	1025-28	000661	1
L2, 3	Inductor, .33μH	DEL	1025-08	000651	2
L4	Inductor, Ferrite Beads, 2ea	EI	0016541		1
Q1, 23	Transistor, 2N3563	FAI	2N3563	003262	3
R1, 10	Resistor, C.C., 51Ω, 1/4W, 5%	AB	CB5105	001076	2
R2	Resistor, C.C., 22K, 1/4W, 5%	AB	CB2235	001120	1
R3, 6	Resistor, C.C., 100Ω, 1/4W, 5%	AB	CB1015	001081	2
R4, 7	Resistor, C.C., 10Ω, 1/4W, 5%	AB	CB1005	001067	2
R5	Resistor, C.C., 2.2K, 1/4W, 5%	AB	CB2225	001103	1
R8	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	1
R9	Resistor, C.C., 150Ω, 1/4W, 5%	AB	CB1515	001083	1

20 MHZ PHASE LOCK OSCILLATOR ASSEMBLY (A1A12)

PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A12	20 MHz Phase Lock Osc. Assy.	EI	34-10733		REF
C1, 2, 6 13, 14	Capacitor, .01μF, 100 WVDC	SPR	TG-S10	000158	5
C3	Capacitor, .005μF	SPR	TG-050	000150	1
C4	Capacitor, .047μF	SPR			1
C5	Capacitor, Variable, 2-8pF	ERR	538-011-NP0-2-8	000339	1
C7	Capacitor, 47pF	SAN	D155F470J0	000065	1
C8, 10, 12 14, 16	Capacitor .001μFd, 100 WVDC	CRL	DD-120	000116	1
C9	Capacitor, 22pF	SAN	D155F220J0	0000050	1
C11	Capacitor, 2pF	SAN	D155F020J0	000026	1
C15	Capacitor, 150pF	SAN	D155F151J0	000084	1
C17	Capacitor, .0015μF	SAN	D195E152J0	000122	1
C18, 19	Capacitor, 1000pF, Feed-thru	CRL	FT 1000	005263	2
CR1	Diode, Varcap Type MV2107	MOT	MV2107	005268	1
E1	P.C. Board	EI	34-09451	049171	1
E2	Cover Assy.	EI	50-09434		
J1, 2	Connector, Coax	SEAL	51-047-0000	000430	2
Q1	Transistor, 2N4124	FAI	2N4124	004791	1
Q2, 3	Transistor 2N3563	FAI	2N3563	003262	3
R1, 9, 15, 16	Resistor, C.C., 4.7K, 1/4W, 5%	AB	CB4725	001109	4
R2	Resistor, C.C., 47K, 1/4W, 5%	AB	CB4735	001124	1
R3	Resistor, C.C., 150K, 1/4W, 5%	AB	CB1545	001133	1
R4, 5	Resistor, C.C., 100K 1/4W, 5%	AB	CB1045	001131	2
R6, 17	Resistor, C.C., 100Ω, 1/4W, 5%	AB	CB1015	001081	2
R7	Resistor, C.C., 150Ω, 1/4W, 5%	AB	CB1515	001083	1
R8	Resistor, C.C., 82K, 1/4W, 5%	AB	CB8235	001129	1

20 MHZ PHASE LOCK OSCILLATOR ASSEMBLY (A1A12)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R10	Resistor, C.C., 6.8K, 1/4W, 5%	AB	CB6825	001113	1
R11, 14, 17	Resistor, C.C., 470Ω	AB	CB4715	001092	3
R12	Resistor, C.C., 390Ω, 1/4W, 5%	AB	CB3915	001091	2
R13, 18	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	2
U1	Intergrated Circuit Type MC4044	MOT	MC4044	005267	1
U2	Intergrated Circuit Type 7490	TI	SN7490	004729	1
U3	Intergrated Circuit Type 74H73/74LS73	TI	SN74LS73	005267	1

IF AMPLIFIER ASSEMBLY (A1A13)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A13	IF Amplifier Assy.	EI	34-11225		REF
C1, 10	Capacitor, 1000pF, Feed-thru	CRL	FT 1000	005263	2
C2, 3, 9	Capacitor, 22μF			004545	3
C4, 5	Capacitor, .15pF, Chip	WEST	SC26BY150K	007132	2
C6, 7	Capacitor, 33pF, Chip	WEST	SC21BY330K	007133	2
E1	P. C. Board	EI	C-11225		1
E2	RF Shield	EI	A-11227	007134	1
E3	Cover Assy.	EI	C-09436	049436	1
J1	Connector, Coax	SEAL	51-047-0000	000430	1
J2	Connector, Coax	SEAL	51-04[illegible]-0000	000428	1
L1	Inductor, 10μH	DEL			1
L2, 3, 4	Inductor, 4 turns #22 AWG, .25" Dia.	EI	A-11224	007131	4
R1	Resistor, C.C., 33Ω, 1/4W, 5%	AB	CB3305	001073	1
R2	Resistor, C.C., 10Ω, 1/4W, 5%	AB	CB1005	001067	1
Rx	Resistor, C.C., 4.7Ω, Nomminal (SAT)	AB	CBXXX5		1
U1 thru 5	Intergrated Circuit Type GPD402	ANA	GPD402	007129	5

AUTO HET PCB ("MOTHER") ASSEMBLY (A1A16)

PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1A16	Auto Het "Mother" Board Assy.	EI	33-10723		REF
E1	P.C. Board	EI	79-10599	006747	1
J1 thru 7	Connector, PCB, 44 pin	CINCH	50-448-10	003505	7
MP1 thru 7	Key, Polarizing PCB	CINCH	50PK2	005048	1
R1	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	1
R2	Resistor, C.C., 3.3K	AB	CB3325	001107	1

COUNTER AND DISPLAY PCB ASSEMBLY (A2)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A2	Counter and Display PCB Assy.	EI	33-09622	33-09622	REF
C1	Capacitor, .01μF, 500 WVDC, 20%		811-Z5V-103P	000168	1
C2	Capacitor, .002μF, 1000 WVDC, Cer.				
C3, 10, 13, 14	Capacitor, .01μF, 100 WVDC, CER. Disc.				
C4	Capacitor, 10μF, 16 WVDC	SPR		006649	1
C5, 6, 9	Capacitor, 220pF, Mica Disc.	SAN	D155F221J0	000089	3
C7	Capacitor, .005μF, Ceramic Disk	SPR	TG-D50	000150	1
C8, 11, 12	Capacitor, 0.1μF, 250 WVDC	AMPE	C280AE/P100K	000211	3
C15, 16	Capacitor, 22μF, 15 WVDC	SPR	198 series	004545	2
CR4, 5	Diode, 1N3605	MOT	1N3605	000550	2
CR6	Diode, Zener	MOT	MZ92-109B	005859	
Q1 thru 11	Transistor, 2N5833	MOT	2N5833	005271	11
Q12 thru 22	Transistor, 2N5400	FAI	2N5400	005233	11
Q23	Transistor, 2N3640	FAI	2N3640	001728	1
Q24, 25, 26 28, 33	Transistor, 2N4124	MOT	2N4124	003294	5
Q27	Transistor, 2N4126	FAI	2N4126	003267	1
Q29	Transistor, 2N4123	MOT	2N4123	003266	1
Q30	Transistor, 2N3440	FAI	2N3440	006259	1
Q31, 32	Transistor, 2N3646	FAI	2N3400	001731	2
R1-18, 42, 44, 64, 75, 76	Resistor, C.C., 3.3KΩ, 1/4W, 5%	AB	CB3325	001107	22
R13	Resistor, C.C., 5.6KΩ, 1/4W, 5%	AB	CB5625	001111	1
R19, 21, 23, 25, 27, 29, 31, 33, 37, 39	Resistor, C.C., 2.2KΩ, 1/4W, 5%	AB	CB2225	001103	11

COUNTER AND DISPLAY PCB ASSEMBLY (A2)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
R20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40	Resistor C.C., 390KΩ, 1/4W, 5%	AB	CB3945	001140	11
R23	Resistor, C.C., 43KΩ, 1/4W, 5%	AB	CB4335	007136	1
R41	Resistor, C.C., 5.6K, 1W, 5%	AB	GB5625	007072	1
R45	Resistor, C.C., 220Ω, 1/2W, 5%	AB	EB2215	001178	1
R49	Resistor, C.C., 56Ω, 1/4W, 5%	AB	CB5605	001077	1
R52, 56, 61, 65, 74, 77	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	6
R53, 55, 59, 66	Resistor, C.C., 10K, 1/4W, 5%	AB	CB1035	001116	4
R57	Resistor, C.C., 10Ω, 1/4W, 5%	AB	CB1005	001067	1
R62, 67	Resistor, C.C., 1.2K, 1/4W, 5%	AB	CB1225	001099	2
R68	Resistor, C.C., 1.8K, 1/4W, 5%	AB	CB1825	001101	1
R70, 73	Resistor, C.C., 330Ω, 1/4W, 5%	AB	CB3315	001090	2
R71, 72	Resistor, C.C., 100Ω, 1/4W, 5%	AB	CB1015	001081	1
R77	Resistor, C.C., 180Ω, 1/4W, 5%	AB	CB1815	001084	2
U1 thru 11, 86	Intergrated Circuit, Type MC836	MOT	MC836P	003613	12
U12, 23, 24, 25, 36, 37, 49, 59	Intergrated Circuit, Type 7451	TI	SN7451	004535	8

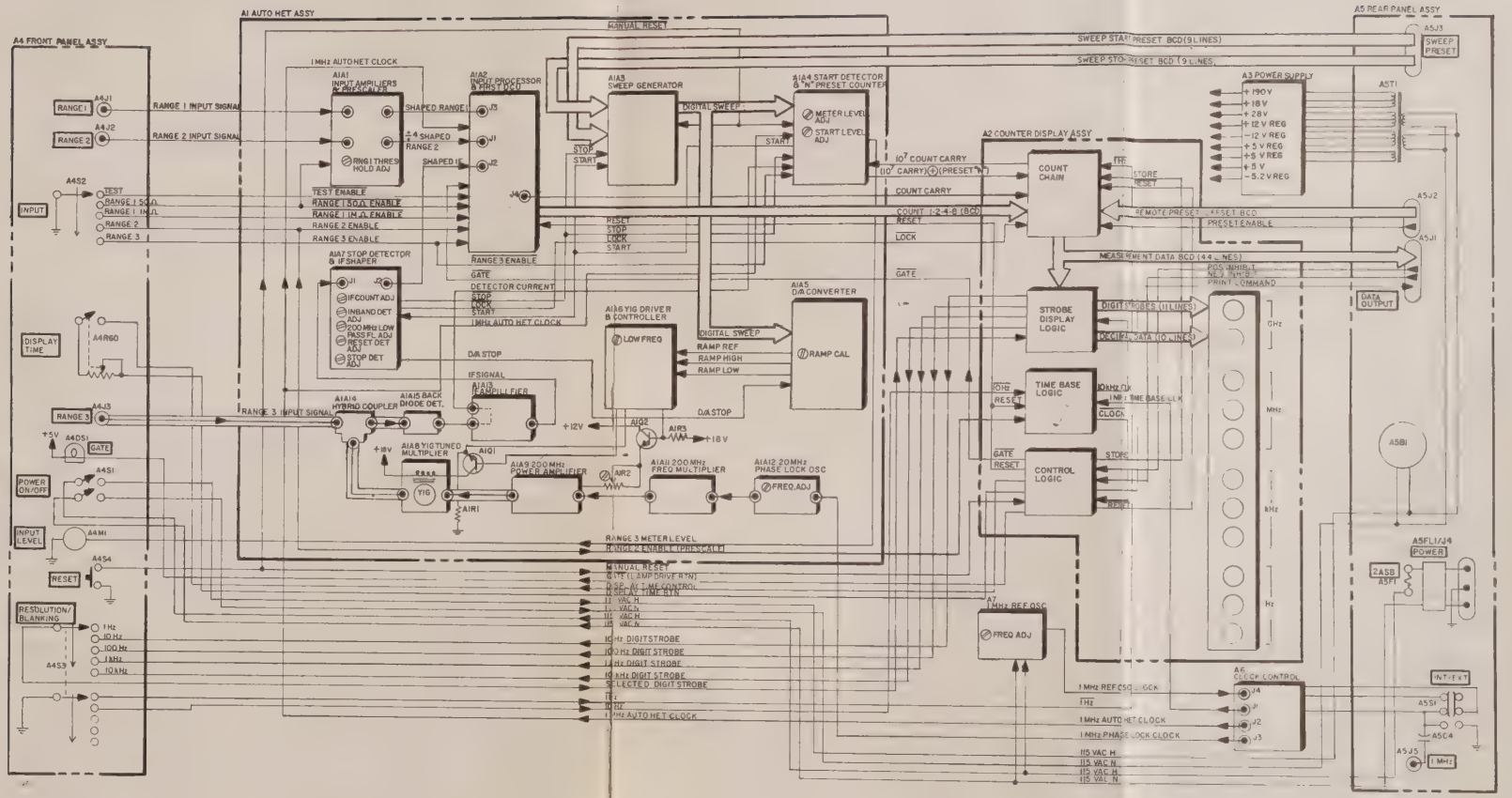


FIGURE 3-1

MODEL 988/989 FUNCTIONAL BLOCK DIAGRAM

COUNTER AND DISPLAY PCB ASSEMBLY (A2)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
U13 thru 22	Intergrated Circuit, Type 74196	TI	SN8280/SN74196	004765	10
U26 thru 30, 32 thru 35, 47, 48	Intergrated Circuit, Type 7475	TI	SN7475	004338	11
U38 thru 46, 54, 55	Intergrated Circuit, Type 7403	TI	SN7403	004517	11
U50	Intergrated Circuit, Type MC3062	MOT	MC3062	004489	1
U51	Intergrated Circuit, Type 7473	TI	SN7473	004776	1
U52, 56, 58	Intergrated Circuit, Type 7404	TI	SN7404	004309	3
U53	Intergrated Circuit, Type 7493	TI	SN7493	004377	1
U60, 69, 70	Intergrated Circuit, Type 7440	TI	SN7440	004524	3
U61	Intergrated Circuit, Type 7442	TI	SN7442	004526	1
U62	Intergrated Circuit, Type 7410	TI	SN7410	004304	1
U63, 67, 73, 76, 79	Intergrated Circuit, Type 7402	TI	SN7402	004303	5
U74	Intergrated Circuit, Type 74121	TI	SN74121	004354	1
U80	Intergrated Circuit, Type 74141	TI	SN74141	004745	1
V1 thru V11	Tube, Display, Nixie 5853	BUR	B5853S	005273	11
XU1 thru 25, 36 thru 44, 46, 49 thru 59, 62 thru 79	Socket, I.C. DIP 14 pin	EI	005107	005107	64

COUNTER AND DISPLAY PCB ASSEMBLY (A2)

PARTS LIST

(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
XU26 thru 35, 47, 48, 61, 80	Socket, I.C. DIP 16 pin	EI	003218	003218	13
XV1 thru 12	Socket, Display Tube	BUR	SK-207	003220	11

POWER SUPPLY ASSEMBLY (A3)

PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A3	Power Supply Assy.	EI	33-10719		REF
C1, 2	Capacitor, 3000μF, 25 WVDC	STM	23C25TS33	067126	2
C3	Capacitor, 25000μF, 35 WVDC	STM		004562	1
C4	Capacitor, 160μF, 40 WVDC	SPR		004232	1
C5	Capacitor, 2μF, 450 WVDC	SPR	150D2224X0020	000255	1
C6, 7	Capacitor, 8000μF, 10 WVDC	ERR	500-1918-01	000327	2
C8, 9, 12, 16, 17	Capacitor, 22μF, 15 WVDC	SPR	198 D series	004545	5
C10, 13, 15	Capacitor, 6.8μF, 35 WVDC	SPR	198 series	000264	3
C11, 14, 18	Capacitor, .22μF, 100 WVDC	SPR	B32232A6224K	000222	3
CR1, 2, 3, 4, 7, 8, 9	Diode, 1N4005	MOT	1N4005	003663	7
CR10, 11, 12, 13	Diode, 1N4997	MOT	1N4997	0003324	4
E1	P. C. Board	EI	79-10499	006748	1
E2	Heat Sink	WAK	672-3-P		1
R1	Resistor, C.C., 470K, 1/4 W, 5%	AB	CB4745	001092	1
R2	Resistor, C.C., 4.7Ω, 1W, 5%	AB	GB47S5	001256	1
R3	Resistor, C.C., 120Ω, 1/2W, 5%	AB	EB1215	001174	1
U2	Intergrated Circuit, Voltage Regulator Type LM 320-K-12	NAT	LM 320-K-12	006770	1
U3	Intergrated Circuit, Voltage Regulator Type LM 320-K-18	NAT	LM 320-K-18	006769	1
U4, 7	Intergrated Circuit, Voltage Regulator, Type LM 309-K	NAT	LM 309-K	006771	2
U5	Intergrated Circuit, Voltage Regulator, Type LM 340-K-12	NAT	LM 340-K-12	006768	1
U6	Intergrated Circuit, Voltage Regulator, Type LM 320-K-5.2	NAT	LM 320-K-5.2	006772	1

FRONT PANEL ASSEMBLY (A4)

PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A4	Front Panel, Assy.	EI	34-09609		REF
A1	Front Sub-Panel Assy.	EI	50-09137	049137	1
A2	Front Dress-Panel Assy.	EI	70-09139	049139	1
CR1	Diode, Signal, 1N695	MOT	1N695	000532	1
DS1	Lamp Assy, Indicator	EI	RODAN 8FK5	005092	1
J1, 2	Connector, Coax, BNC, UG1094	AML	UG1094	004903	2
J3	Connector, Coax, Type N	EI	A753S-3DB	006758	1
M1	Meter, Level	EI	99-09194	006791	1
MP1	Bracket, Mounting Center rail	EI	B-11245	007151	1
MP2	Lens, Display	EI	50-09444	049444	1
MP3, 4	Knob, Control	NBX	126	003082	2
MP5	Knob, Control	NBX	1-103	003083	1
MP6	Knob, Control	NBX	125	003435	1
S1	Switch, Rotary, DPST	AH	AH81727	006757	1
S2, 3	Switch, Waffer, 5 position	CTS	T-206 series	001567	2
S4	Switch, Push Button	GH	1591811	001583	1
S5	Switch, SPST W/	CTS	SB-3796A	001012	1
R60	1 Meg. Potentiometer				

REAR PANEL ASSEMBLY (A5)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A5	Rear Panel Assy.	EI	34-09610		REF
A1	Rear Panel (Blank)	EI	50-09178	009178	1
B1	Blower, Fan Assy	EI		003068	1
C4	Capacitor, .01μF, Disk	SPR	RMC-Z5U	000169	1
F1	Fuse, 2 Amp., SB, 3AG	LTTL	313.002	000607	1
FL1/J4	Line Filter/Connector	EI		003333	
J1	(See Option P Parts List)				REF
J2	(See Option J Parts List)				REF
J3	(See Option S Parts List)				REF
J5	Connector, BNC, UG1094	AML	UG1094	004903	1
J6, 7, 8	(See Option N Parts List)				REF
MP1, 2	Cover Plate, Connector 50 pin	EI	50-05398	045598	2
MP3	Cover, Plate, "N" Opt.	EI	50-09180	049180	1
MP4	Cover, Plate, Connector, 24 pin	EI	50-09182	049182	1
S1	Switch, Slide	SWT	46206LFR	001554	1
S2	Switch, Slide	SWT	46256LFR	001588	1
T1	Transformer, Power	EI	95-09188	049188	1
XF1	Holder, Fuse	LTTL	432014	005774	1

CLOCK CONTROL PCB ASSEMBLY (A6)
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A6	Clock Control Assy.	EI	33-10720		REF
C1	Capacitor, .22μF	EI		005815	1
C2	Capacitor, 22μF, 15 WVDC	SPR	198 D series	004545	1
E1	P. C. Board	EI	79-10721	006786	1
J1 thru 4	Connector,	SEAL	51-051-0000	000432	4
Q1	Transistor, 2N3646	MOT	2N3646	001731	1
R1	Resistor, C.C., 470Ω, 1/4W, 5%	AB	CB4715	001092	1
R2	Resistor, C.C., 2.7K, 1/4W, 5%	AB	CB2725	001105	1
R3	Resistor, C.C., 3.3K, 1/4W, 5%	AB	CB3325	001107	1
R4	Resistor, C.C., 47Ω, 1/4W, 5%	AB	CB4705	001731	1
R6	Resistor, C.C., 10K, 1/4W, 5%	AB	CB1025	001116	1
R9	Resistor, C.C., 1K, 1/4W, 5%	AB	CB1025	001098	1
U1	Intergrated Circuit, Type MC309H	MOT	MC309H	006766	1
U2	Intergrated Circuit, Type SN7490	TI	SN7490P	004729	1
U3	Intergrated Circuit, Type MC3008	MOT	MC3008P	004485	1

MODEL 988A/989A TOP ASSEMBLY
PARTS LIST

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
A1	Auto Het Assembly	EI	34-10715		1
A2	Counter and Display PCB Assy.	EI	33-09622		1
A3	Power Supply PCB	EI	33-10719		1
A4	Front Panel Assy.	EI	34-09609		1
A5	Rear Panel Assy.	EI	34-09610		1
A6	Clock Control Assy.	EI	33-10720		1
A7	1MHz Reference Osc. Assy.	OVEN	22-16-B	003291	1
A7C1, 2	Capacitor .001μF, 100 WVDC	CRL	DD-120	000117	2
A7C3	Capacitor .1μF, 250 WVDC	AMPE	C280AE/P100K	000211	1
MP1	Right side sub-panel	EI	D-09367	049367	1
MP2	Right side dress-panel	EI	C-10770	006796	1
MP3	Left side sub-panel	EI	D-09370	049370	1
MP4	Left side dress-panel	EI	C-10769	006795	1
MP5	Center Rail	EI	D-11237	007153	1
MP6	Top Cover	EI	D-10767	0067971	1
MP7	Bottom Cover	EI	D-10768	006798	1
MP8	Brace, Display PCB	EI	B-10817	006794	1
MP9	Bracket, Display	EI	B-09448	006793	1
MP10	Bracket, Mounting Counter and Display Assy.	EI	B-09371	094371	1
MP11	Bracket, Osc. mounting and Heat sink support	EI	C-11145	007110	1
MP12, 16	Handle, Instrument	EI	C-09432	049432	2
MP13	Spacer, Power Transformer	EI	A-11238	007152	1
MP14	Bail, Mount with feet, 12"	EI		003077	1
MP15	Handle, Carrying	EI		000625	1
W1	Cable, Line Cord, Detachable	EI	A-09226	049226	1
W2	Cable Assy., Coax	EI	B-10830		1
W3	Cable Assy., Coax	EI	B-10831		1
W4	Cable Assy., Coax	EI	B-10834		1
W5	Cable Assy., Coax	EI	B-10837		1
W6	Cable Assy., Coax	EI	B-11024		1

MODEL 988A/989A TOP ASSEMBLY
PARTS LIST
(Continued)

Reference	Description	Mfr.	Mfr. No.	EI No.	Qty.
W7	Cable Assy., Coax	EI	B-11026		1
W8	Cable Assy., Coax	EI	B-11027		1
W9	Cable Assy., Coax	EI	B-11029		1
W10	Cable Assy., Coax	EI	B-11251		1
W11	Cable Assy., Coax	EI	B-11252		1
W12	Cable Assy., Coax	EI	B-10839		1

SECTION 6

SCHEMATICS AND RELATED DRAWINGS

SECTION 6

SCHEMATICS AND RELATED DRAWINGS

This section contains the schematic and component location diagrams of the Model 988/989 Microwave Counter. The schematic diagram appears on the foldout sheet while the corresponding component location diagram appears on the left hand page opposite the schematic, for all the functions located on assemblies A1, A3 and A6. The schematic diagrams of the functions located on assembly A2 are supported by figure 6-19 the counter/display PCB assembly (A2) component location diagram. If further component information is required, consult the individual assembly parts list contained in Section 5 of this manual. Table 6-1 lists the schematic and component location diagrams by figure number, and provides the functional circuit and/or assembly name and the E.I. drawing number when applicable.

TABLE 6-1

LIST OF SCHEMATIC AND COMPONENT LOCATION DIAGRAMS

FIG. #	ASSEMBLY AND/OR CIRCUIT FUNCTIONAL NAME	E.E. DWG. #
6-1	Time Base Logic (P/O A2), Schematic Diagram.	D-11-09585
6-2	Clock Control Assembly (A6), Schematic and Component Location Diagram.	C-11-10822
6-3	Control Logic (P/O A2), Schematic Diagram.	D-11-09582
6-4	Count Chain (P/O A2), Schematic Diagram.	D-11-09587
6-5	Strobe Display Logic (P/O A2), Schematic Diagram.	D-11-10123
6-6	Range 1 and 2 Input Amplifiers and Prescaler Assembly (A1A1), Schematic and Component Location Diagram.	C-11-10732
6-7	Input Control and 1st DCU Assembly (A1A2), Schematic and Component Location Diagram.	D-11-10850
6-8	Sweep Generator Assembly (A1A3), Schematic and Component Location Diagram.	D-11-09473
6-9	Start Detector and Preset "N" Counter Assembly (A1A4), Schematic and Component Location Diagram.	D-11-09470
6-10	Digital - to - Analog Converter Assembly (A1A5), Schematic and Component Location Diagram.	D-11-09474
6-11	YIG Driver/Controller Assembly (A1A6), Schematic and Component Location Diagram.	D-11-09570
6-12	Stop Detector and IF Shaper Assembly (A1A7), Schematic and Component Location Diagram.	D-11-10725

TABLE 6-1

Continued

FIG #	ASSEMBLY AND/OR CIRCUIT FUNCTIONAL NAME	E.E. DWG. #
6-13	200 MHz Power Amplifier Assembly (A1A9), Schematic and Component Location Diagram.	C-11-09471
6-14	200 MHz Frequency Multiplier Assembly (A1A11), Schematic and Component Location Diagram.	C-11-09469
6-15	20 MHz Phase Lock Oscillator Assembly (A1A12), Schematic and Component Location Diagram.	C-11-09450
6-16	If Amplifier Assembly (A1A13), Schematic and Component Location Diagram.	C-11-11182
6-17	Power Supply Assembly (A3), Schematic and Component Location Diagram.	C-11-10722
6-18	Auto Het Assembly (A1) Component Location Diagram.	
6-19	Counter/Display PCB Assembly (A2), Component Location Diagram.	
6-20	Front Panel Assembly (A4), Component Location Diagram.	
6-21	Rear Panel Assembly (A5), Component Location Diagram.	
6-22	Model 988/989 Interconnect Schematic Diagram.	

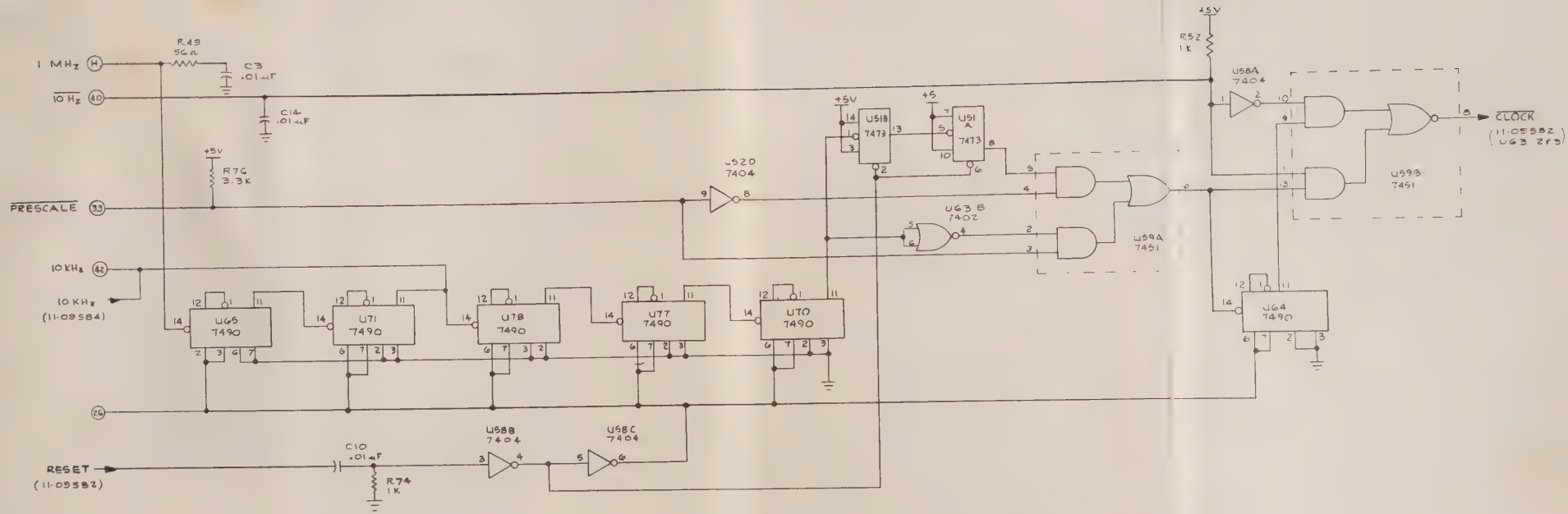
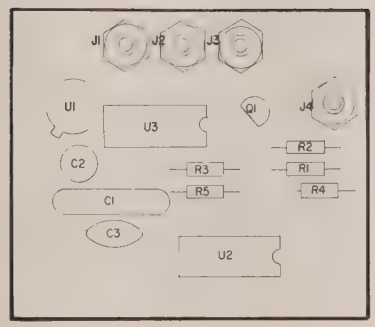
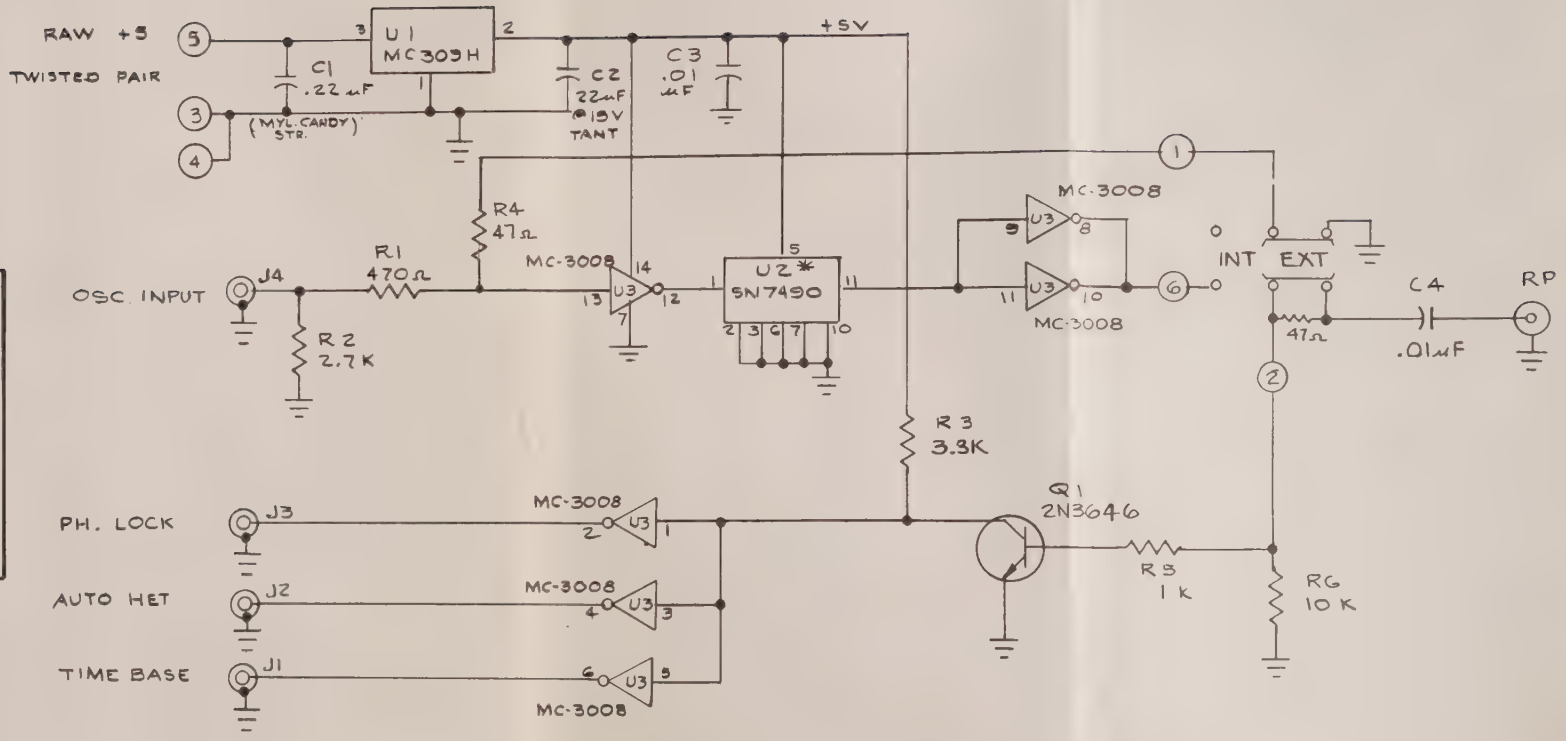


FIGURE 6-1
TIME BASE LOGIC (P/O A2),
SCHEMATIC DIAGRAM
(D-11-09585)





NOTES:

1. USED ONLY ON OPTIONS 'D' & 'E', IN STANDARD UNIT JUMPER (SLEEVE BUSS) PINS 1 TO 11.

FIGURE 6-2
CLOCK CONTROL ASSEMBLY (A6), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(C-11-10822)

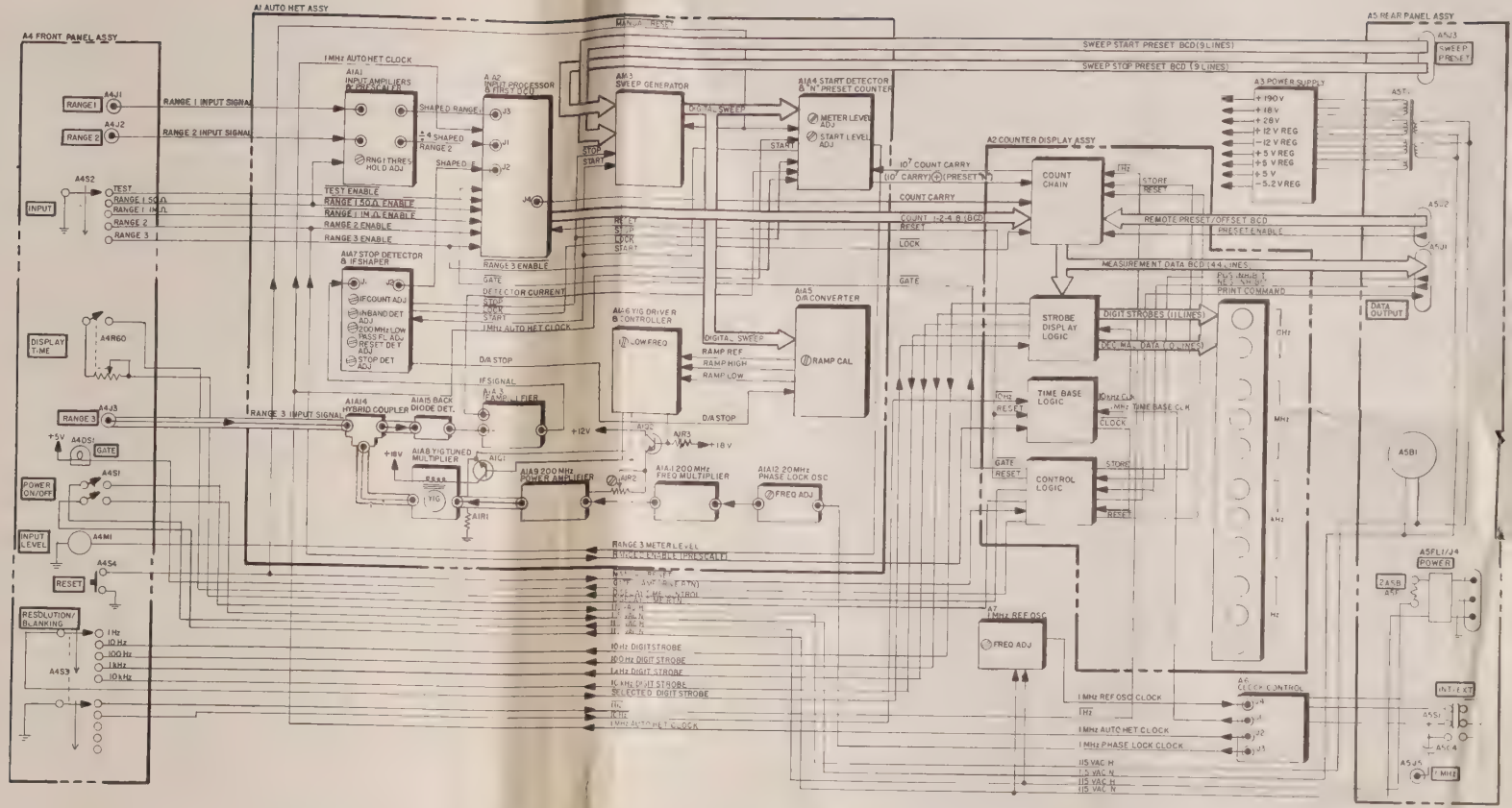


FIGURE 3-1

MODEL 988/989 FUNCTIONAL BLOCK DIAGRAM

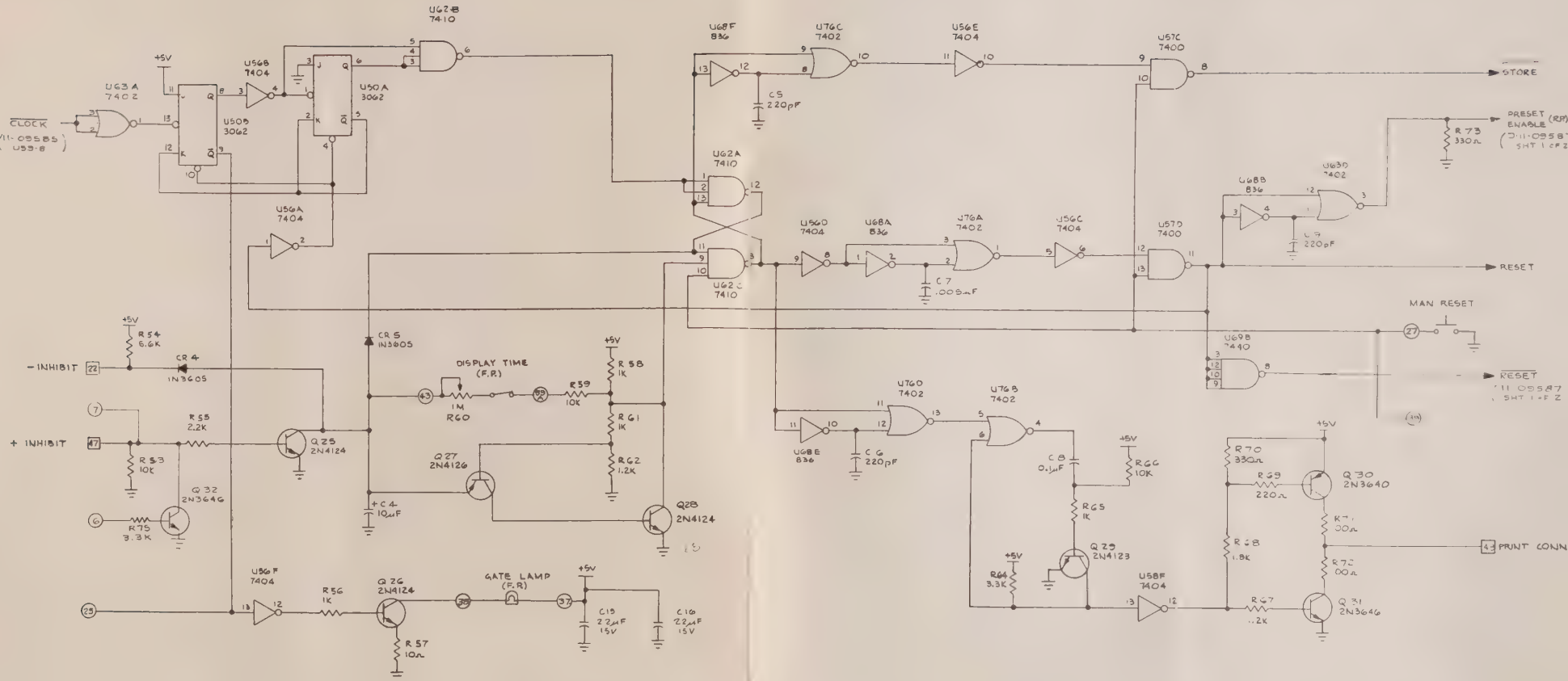


FIGURE 6-3
CONTROL LOGIC (P/O A2),
SCHEMATIC DIAGRAM
(D-11-09582)

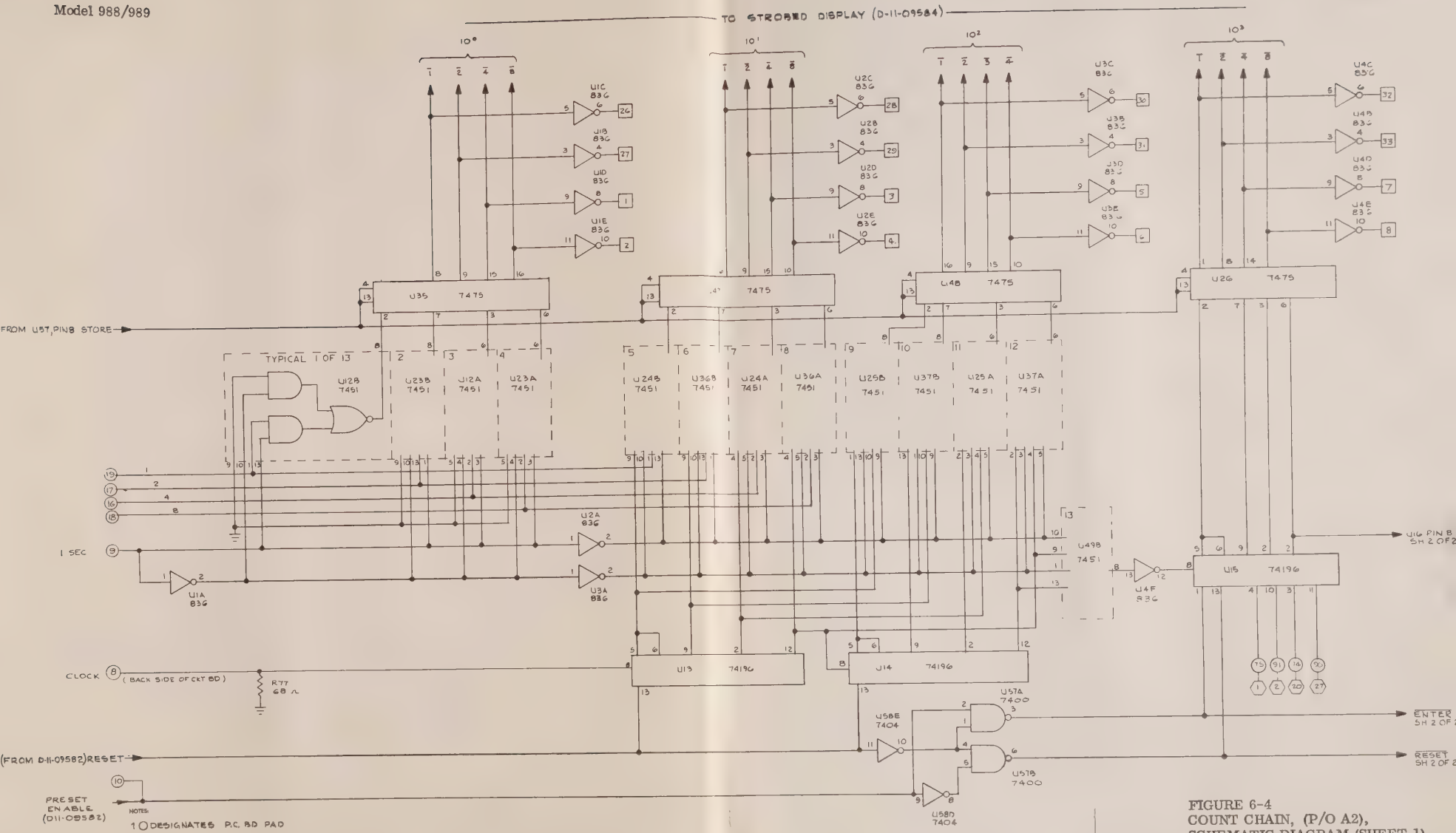
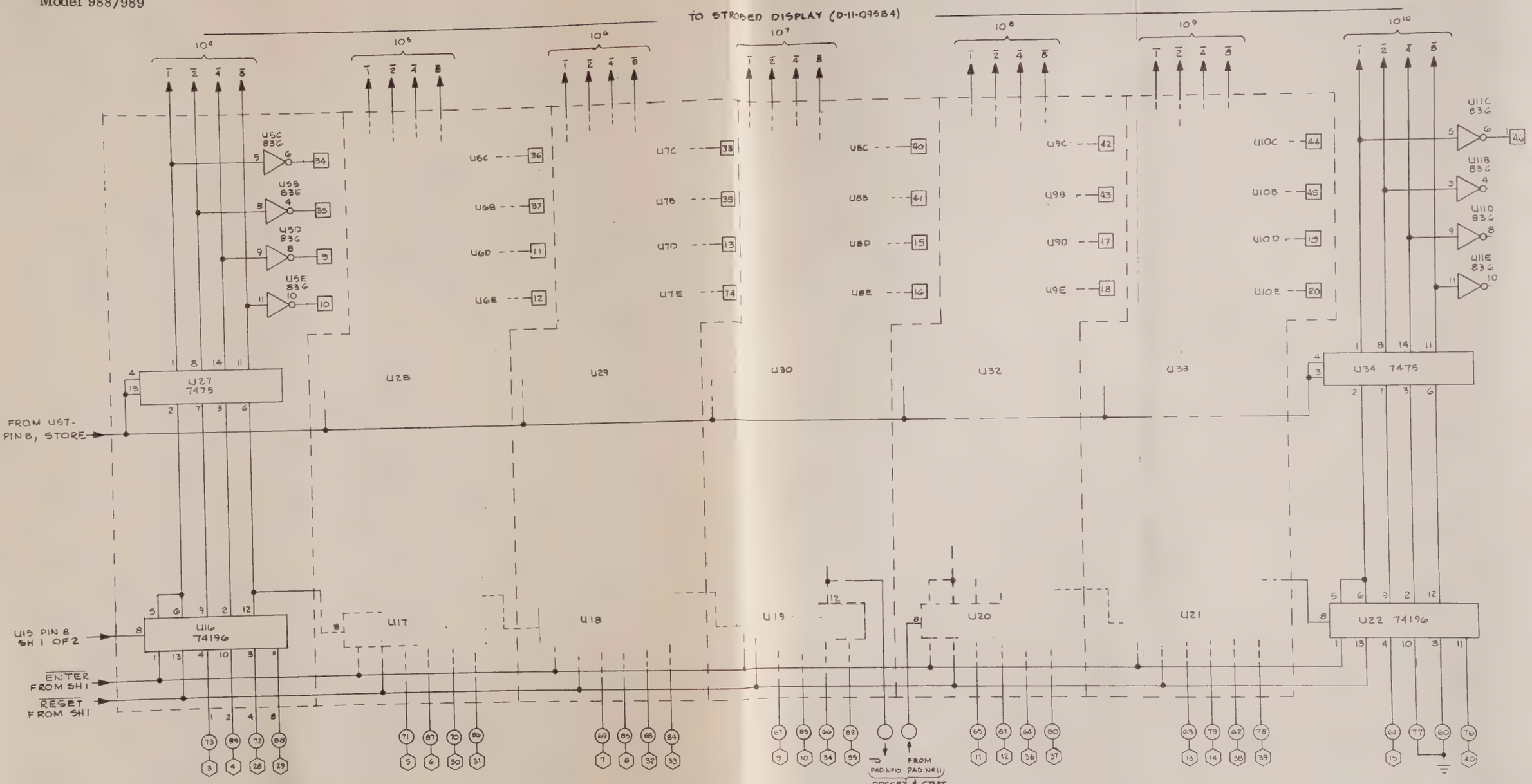


FIGURE 6-4
COUNT CHAIN, (P/O A2),
SCHEMATIC DIAGRAM (SHEET 1)
(D-11-09587 SHEET 1)



NOTES:
SEE SHT 1

FIGURE 6-4
COUNT CHAIN, (P/O A2),
SCHEMATIC DIAGRAM (SHEET 2)
(D-11-09587 SHEET 2)

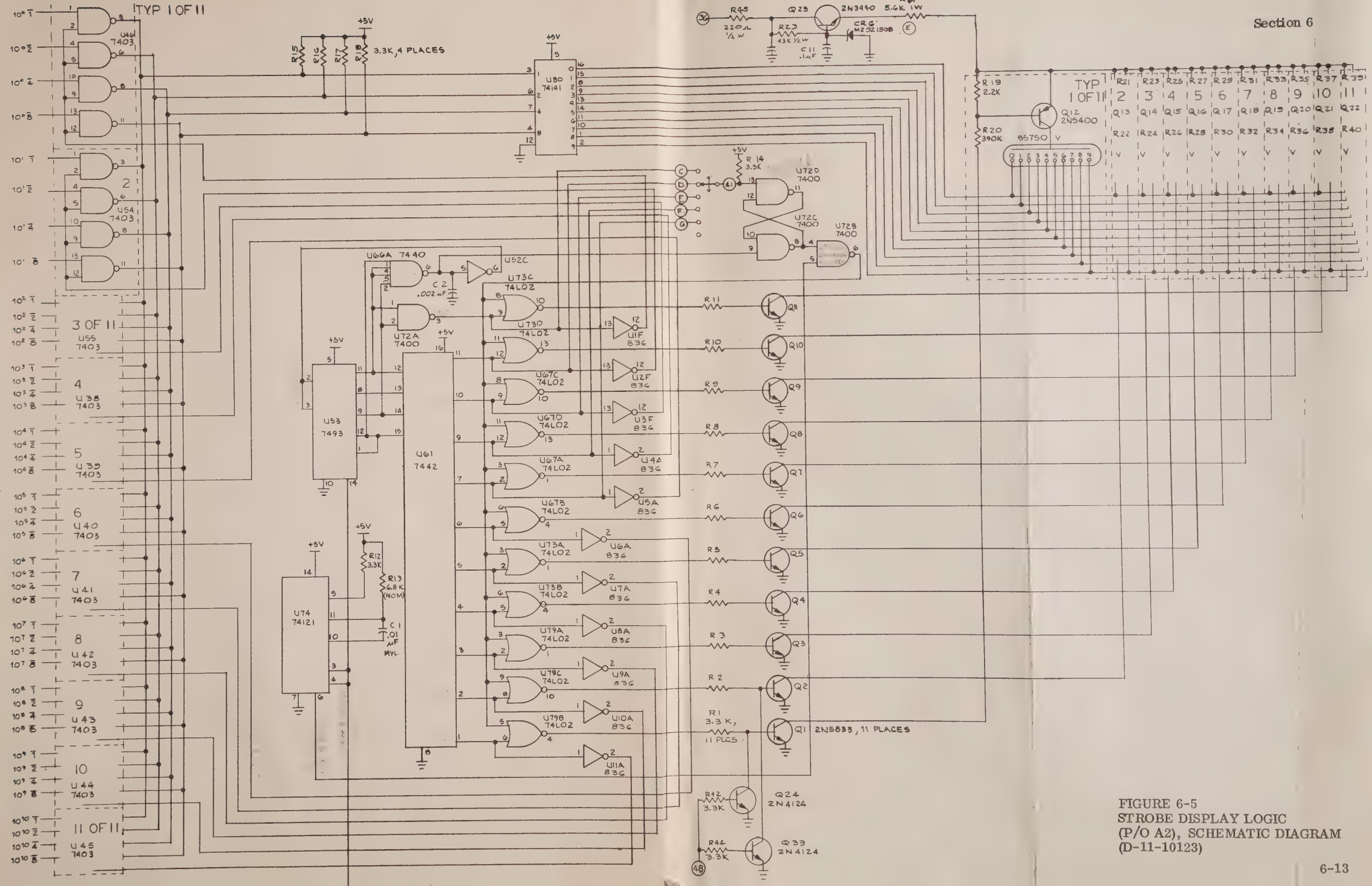
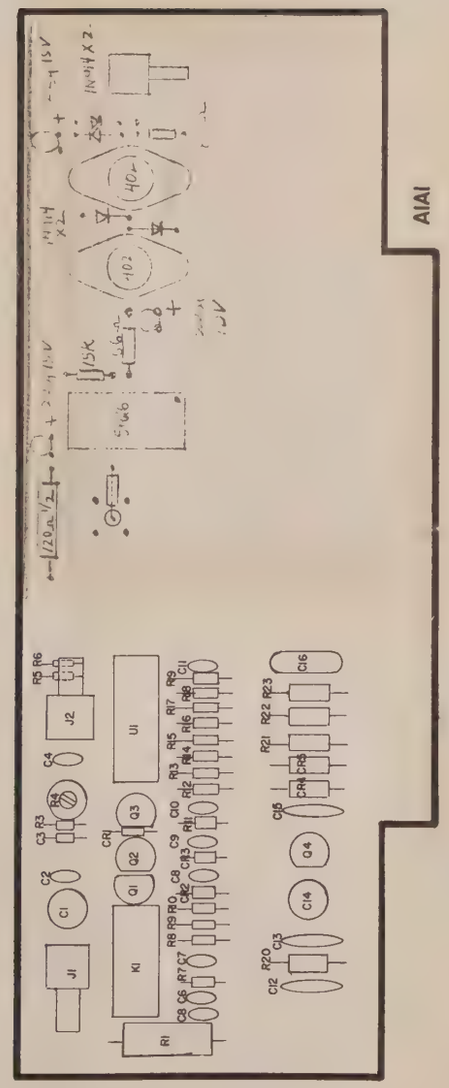
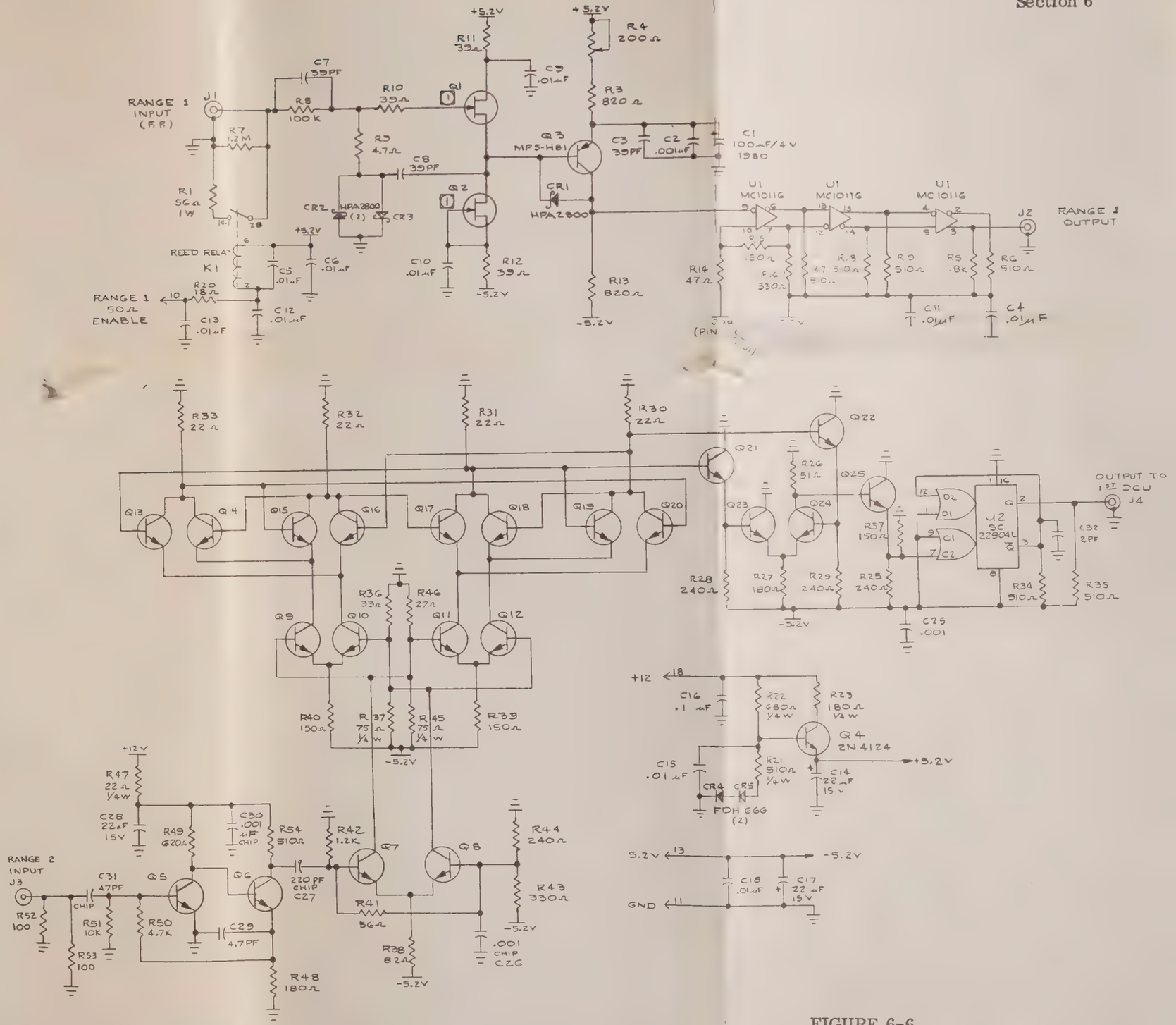


FIGURE 6-5
STROBE DISPLAY LOGIC
(P/O A2), SCHEMATIC DIAGRAM
(D-11-10123)

D-11-09587 SHT 2 OF 2





NOTE:

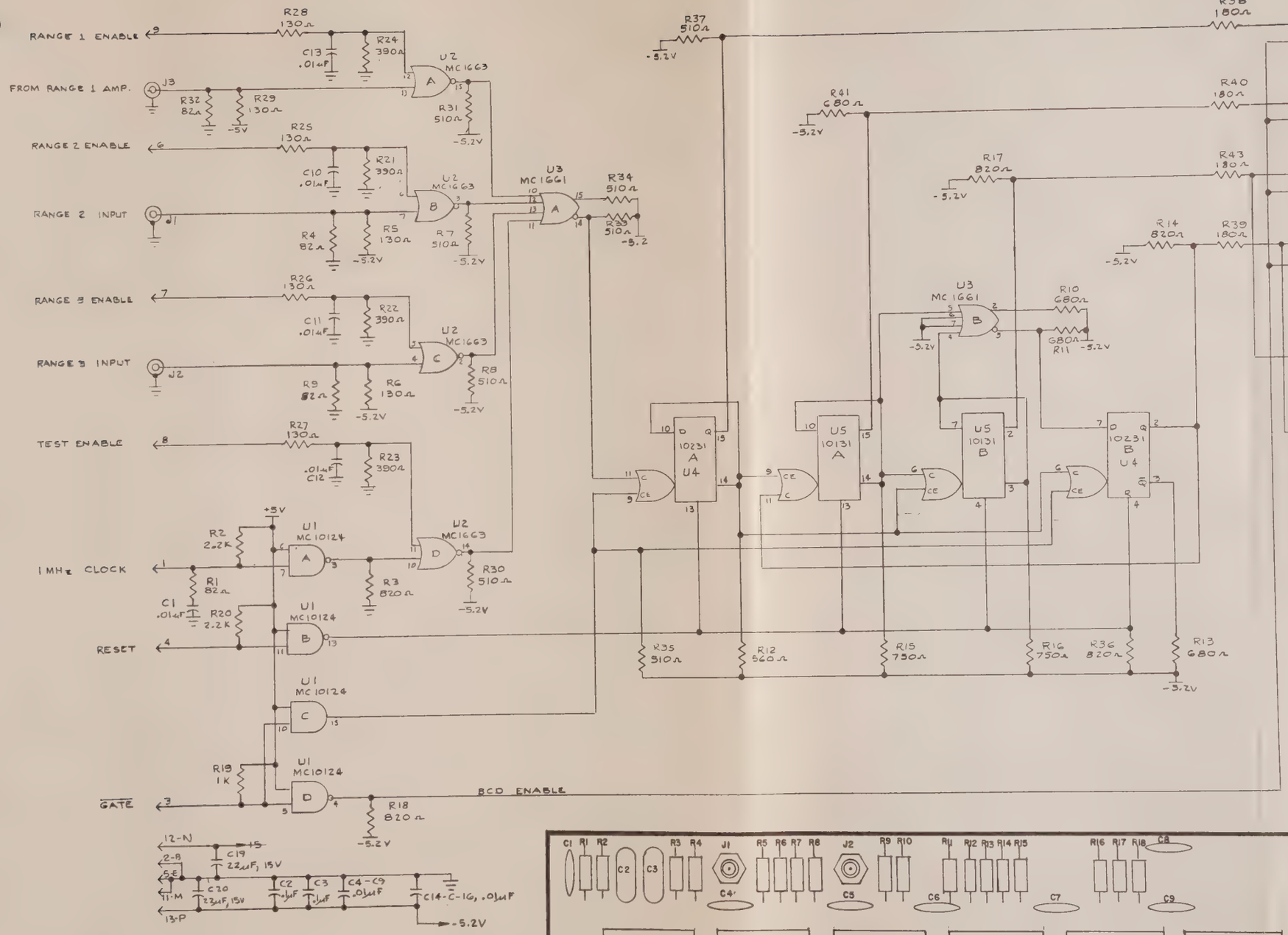
1. Q1 & Q2 ARE SELECTED

Q5 & Q6 ARE MMT 8015, ALL OTHER TRANSISTORS ARE MMT 3960

UNLESS NOTED ALL RESISTOR ARE 1/8W.

REF.- 300 Ma POWER DRAIN. -5.2V SUPPLY

FIGURE 6-6
RANGE 1 AND 2 INPUT AMPLIFIERS AND PRESCALER ASSEMBLY (A1A1), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
C-11-10732



NOTES:

1. ALL RESISTORS 1/4 W
2. BYPASS 10124 +5 W/ .1 μF & -5 W/ .1 μF CAP.
3. BYPASS 10131, 10231, 1661, 10115 & 1039 +5V & -5V W/ .01 μF CAP.

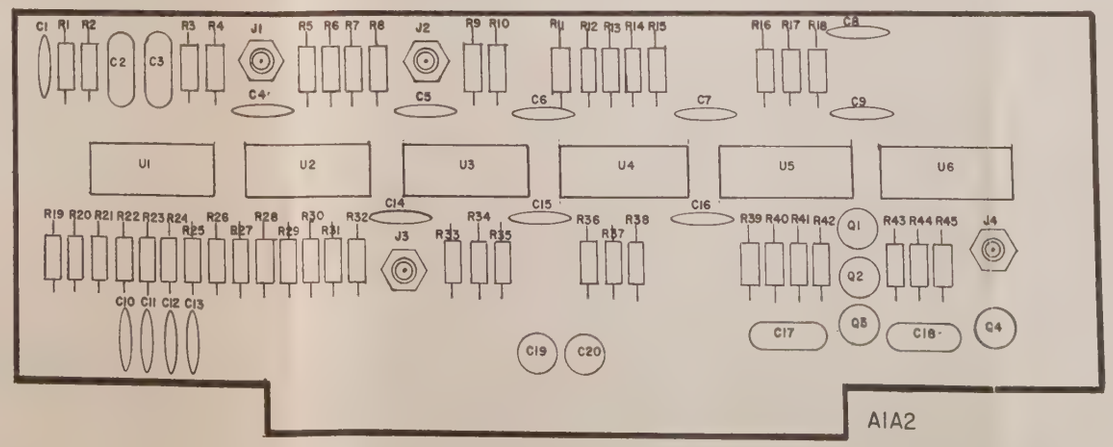
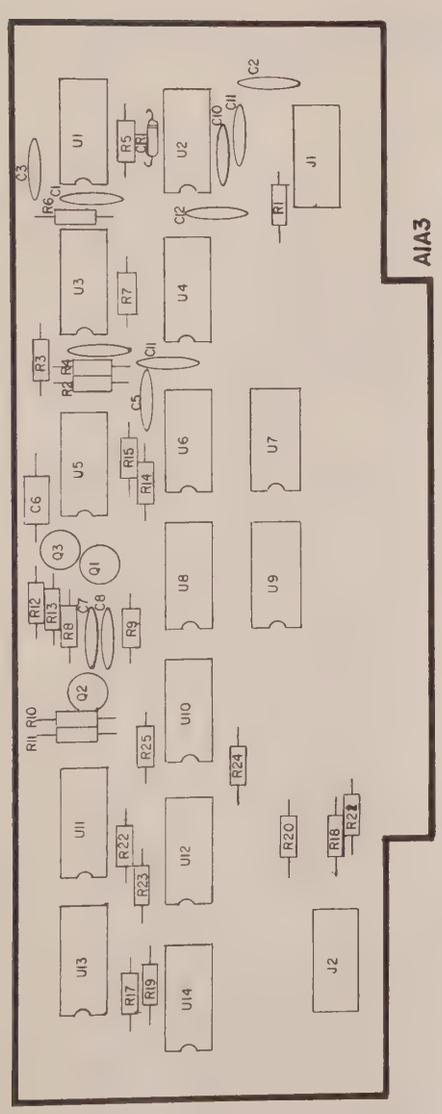


FIGURE 6-7
INPUT CONTROL AND 1ST DCU ASSEMBLY (A1A2), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(D-11-10850)



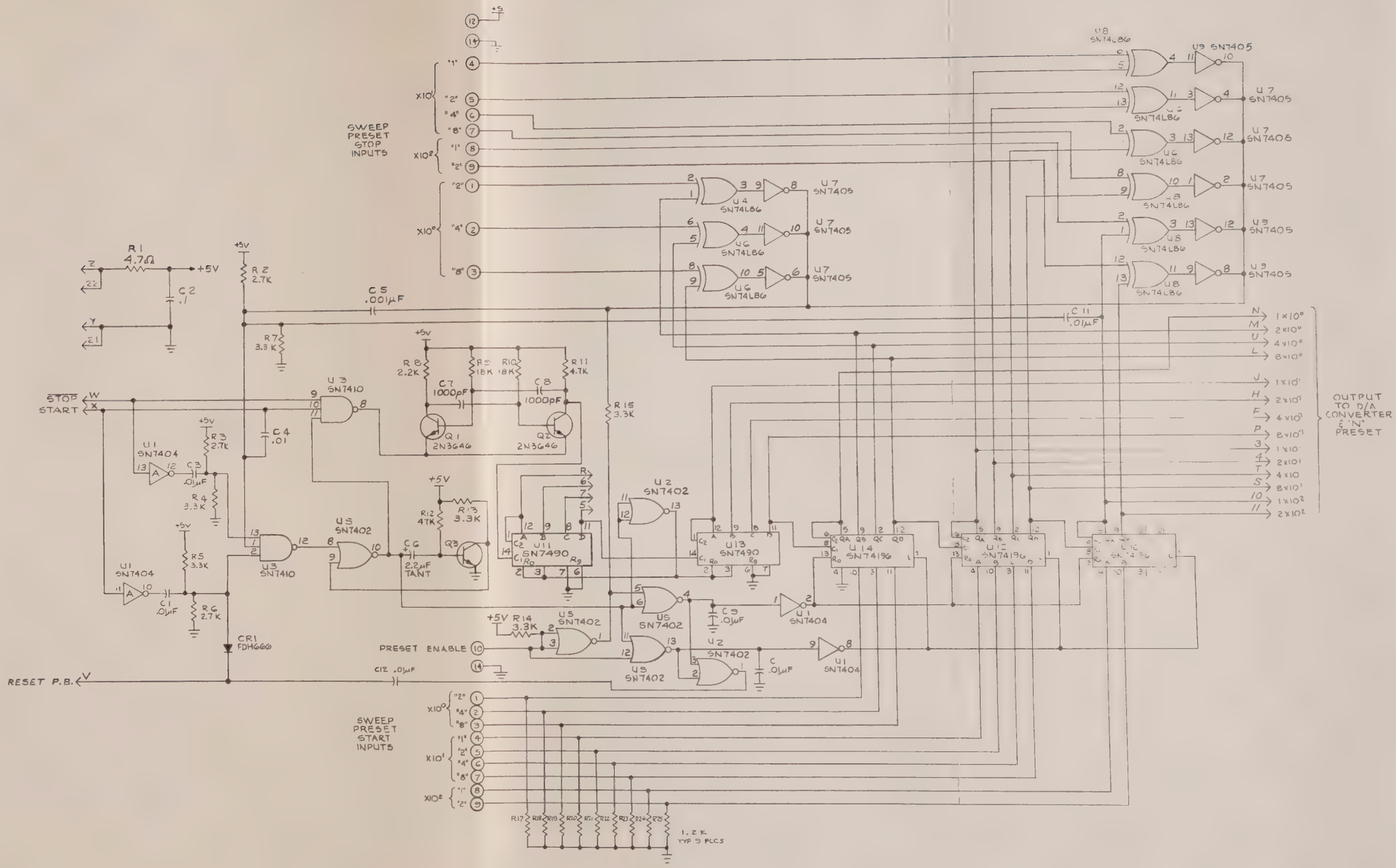
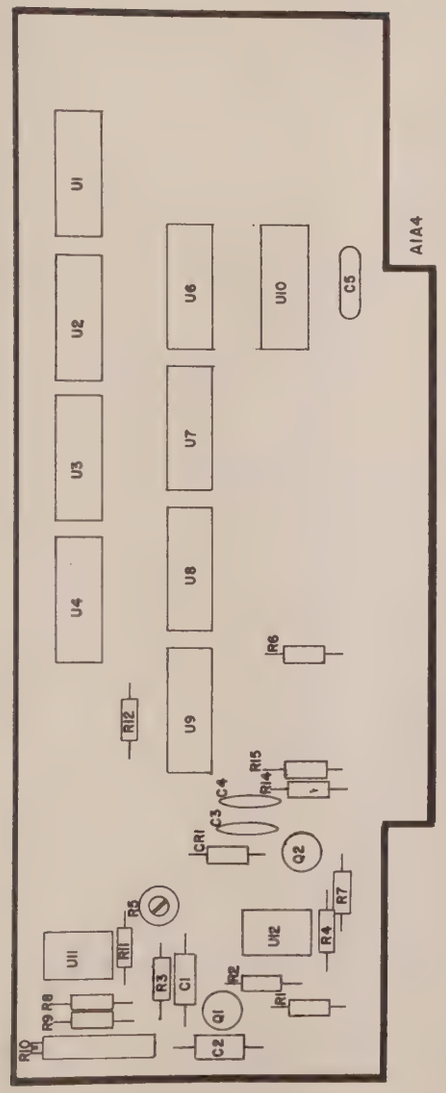
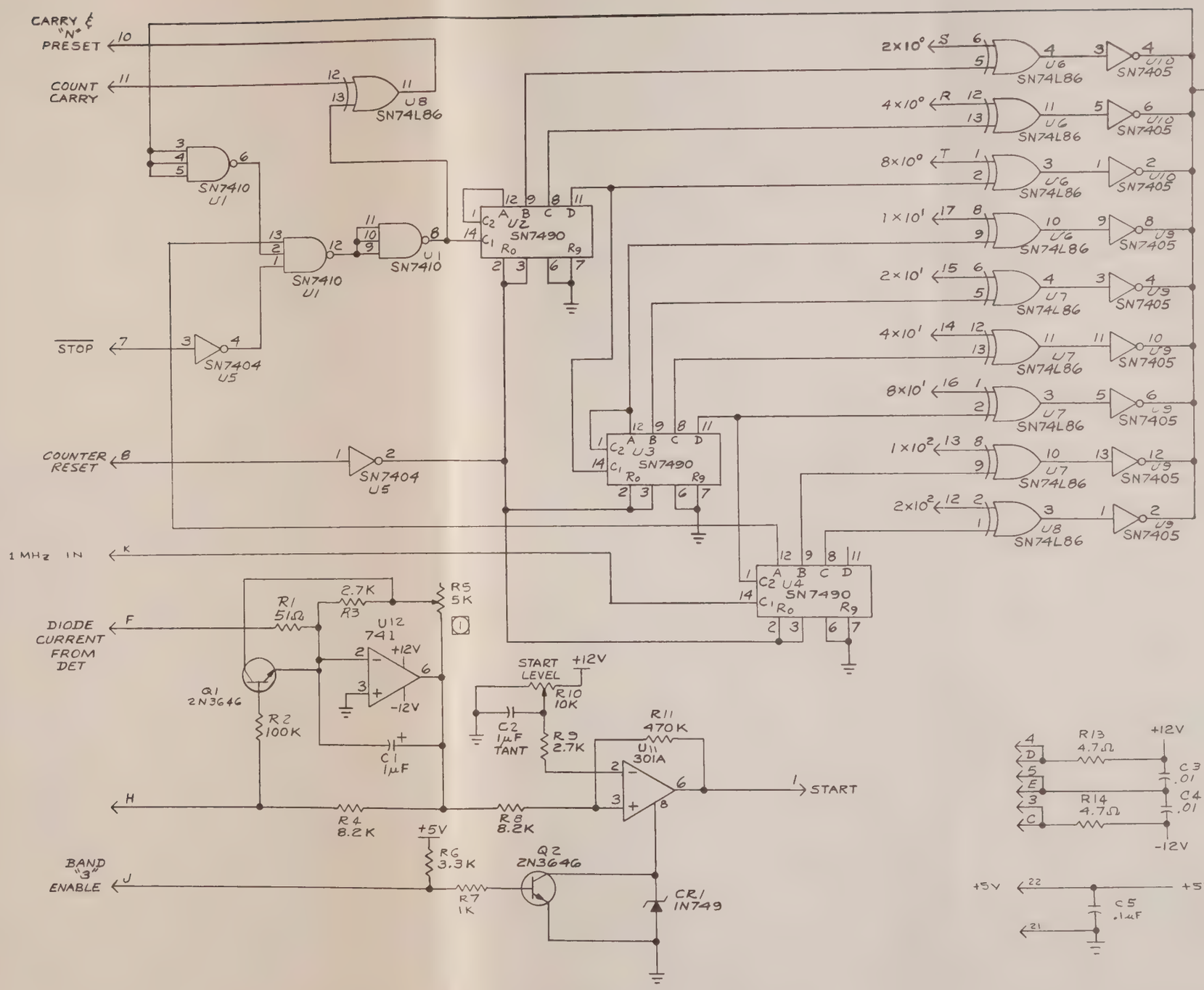


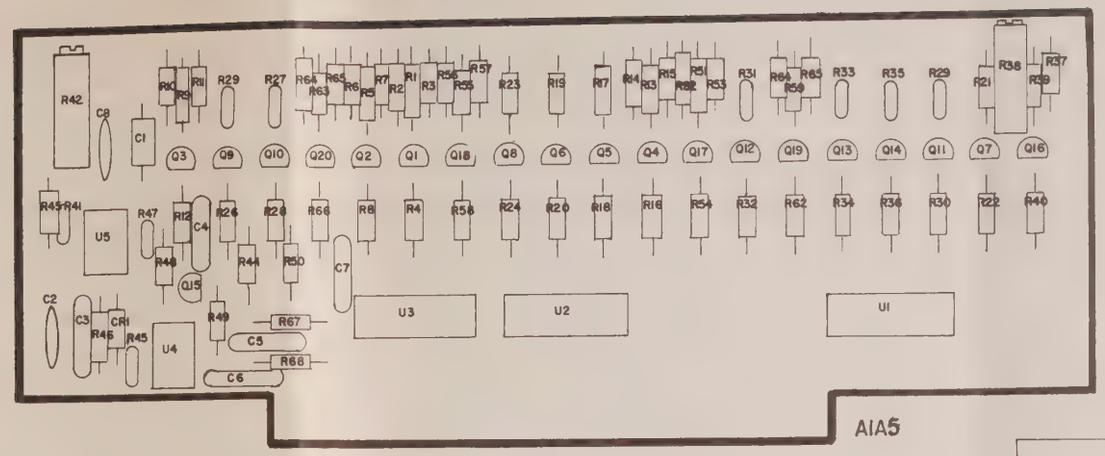
FIGURE 6-8
SWEEP GENERATOR ASSEMBLY (A1A3), SCHEMATIC AND COMPONENT LOCATION DIAGRAM (D-11-09473)





START DETECTOR

FIGURE 6-9
START DETECTOR AND PRESET "N" COUNTER ASSEMBLY (A1A4), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(D-11-09470)



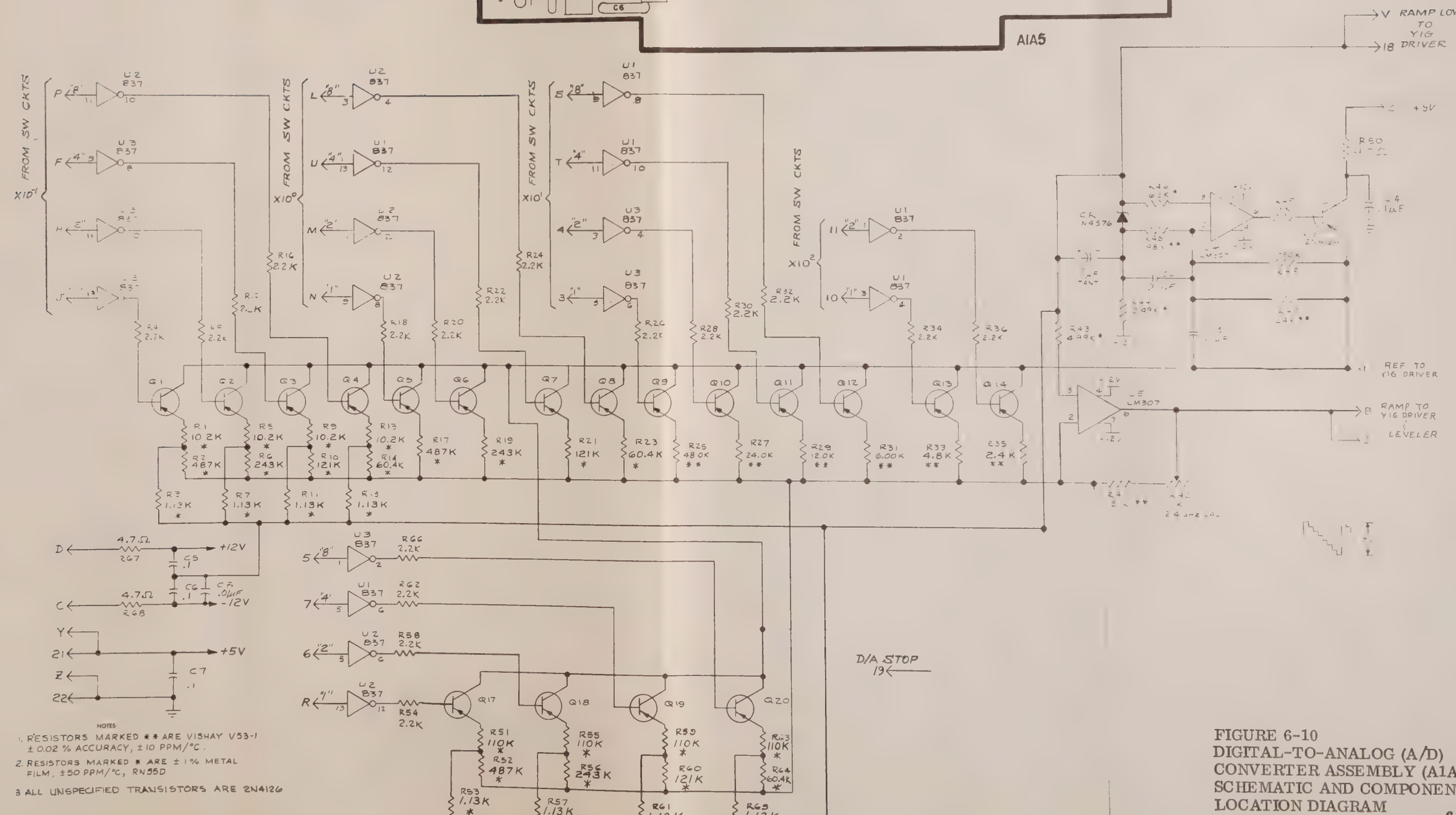
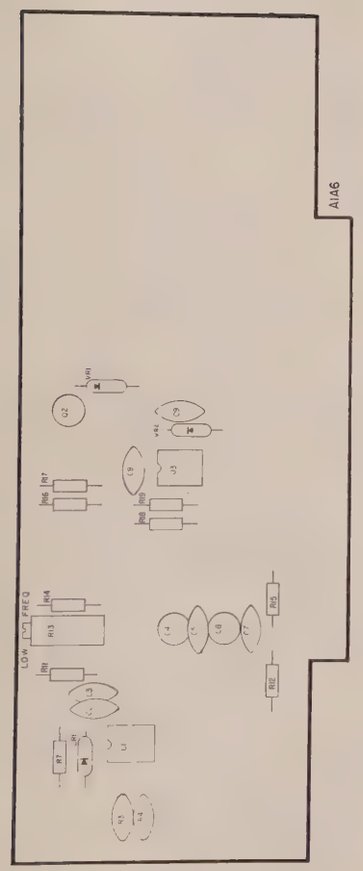


FIGURE 6-10
DIGITAL-TO-ANALOG (A/D) CONVERTER ASSEMBLY (A1A5), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(D-11-09474)



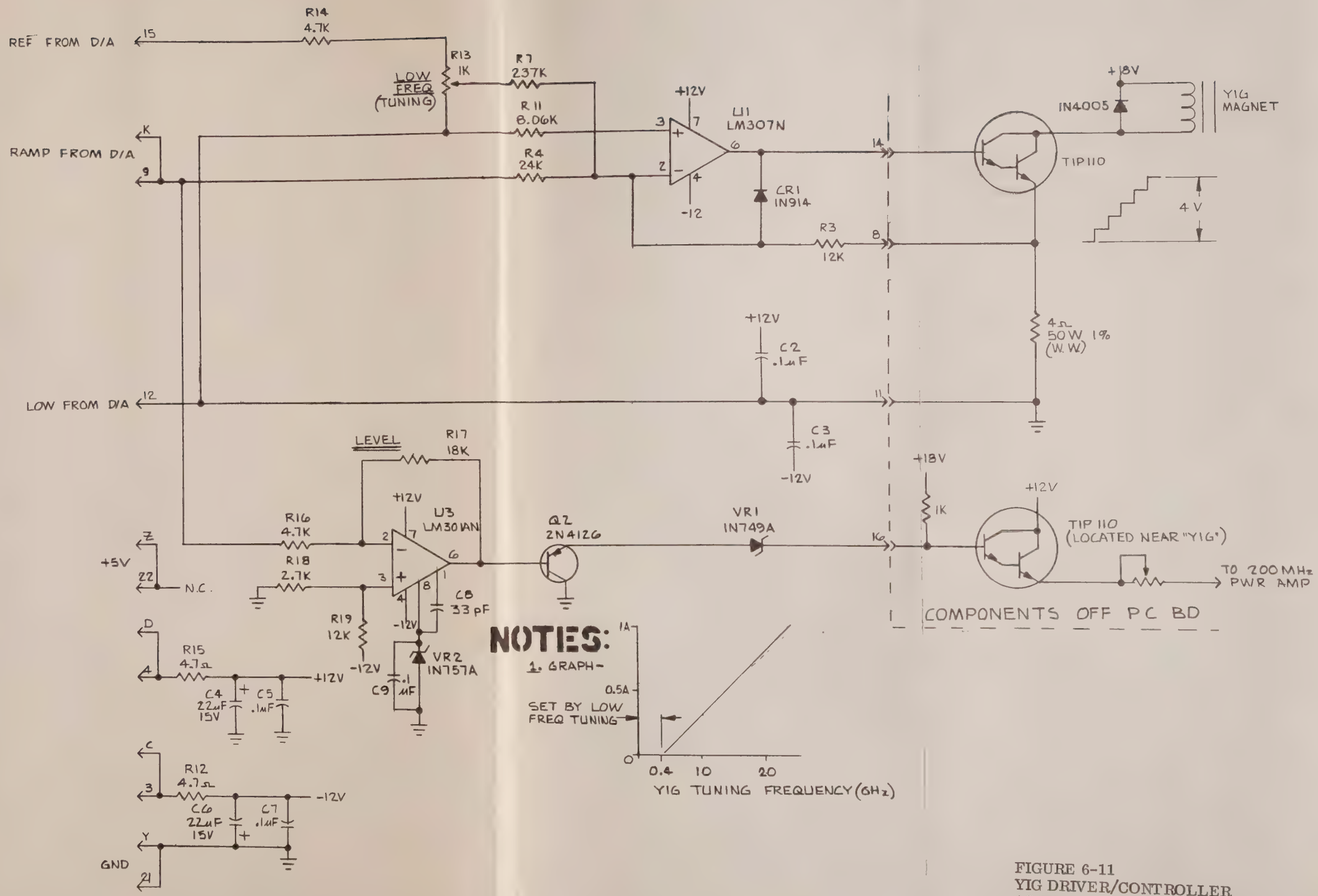
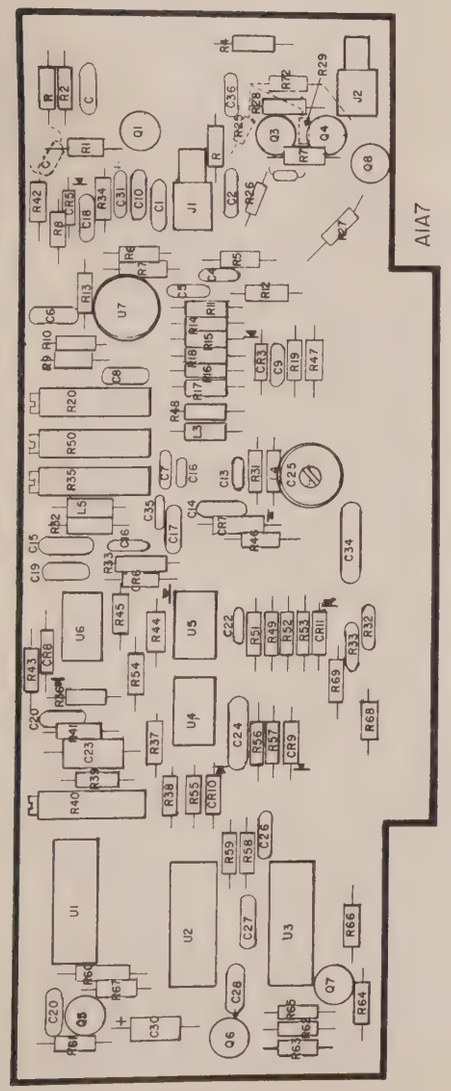


FIGURE 6-11
YIG DRIVER/CONTROLLER
ASSEMBLY (A1A6), SCHEMATIC
AND COMPONENT LOCATION
DIAGRAM
(C-11-11210)



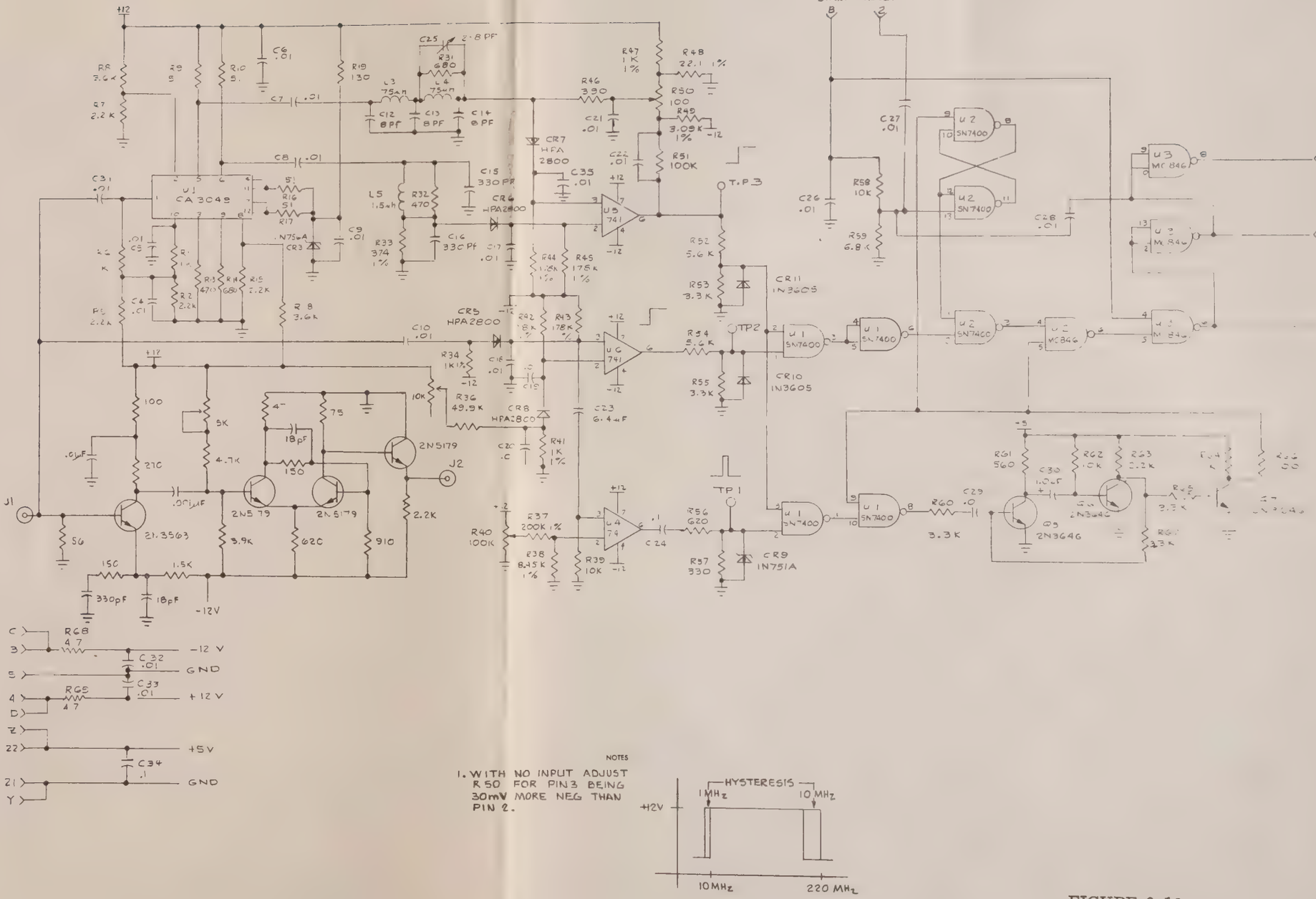
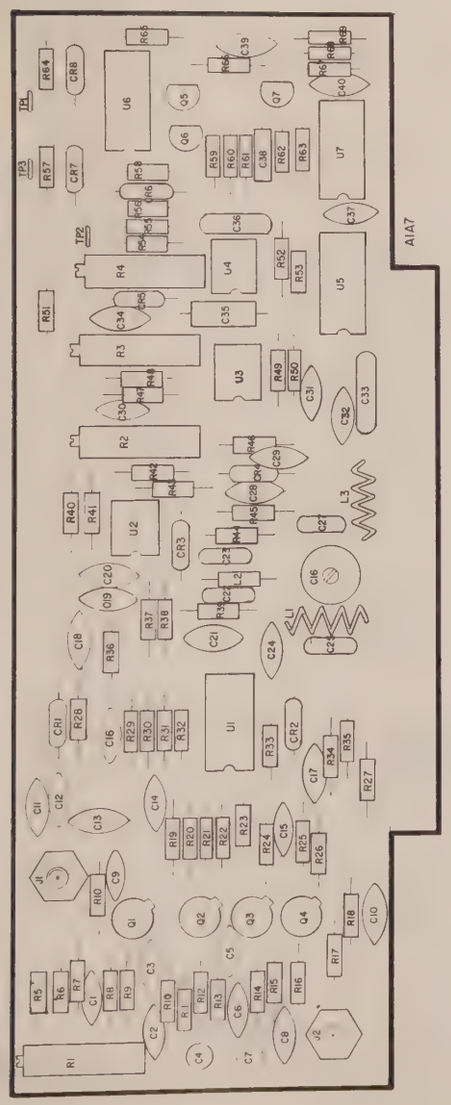


FIGURE 6-12
STOP DETECTOR AND IF SHAPER ASSEMBLY (A1A7), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(D-11-10725)



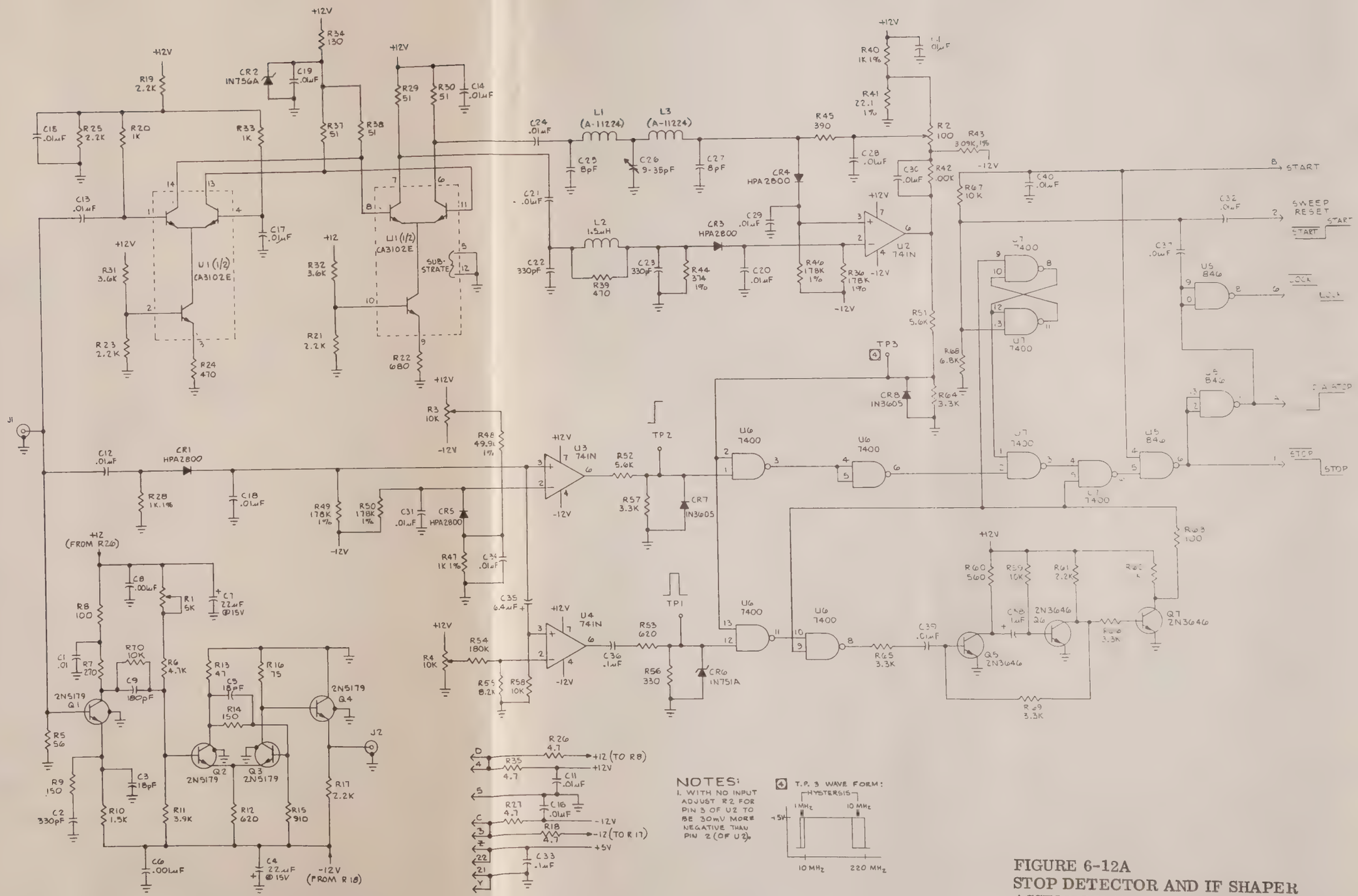
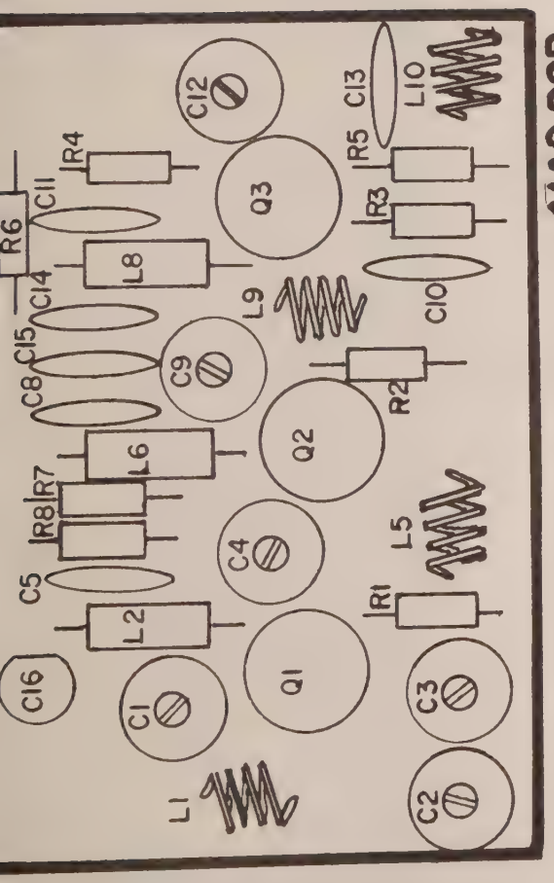


FIGURE 6-12A
STOP DETECTOR AND IF SHAPER ASSEMBLY (A1A7), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(D-11-10725)



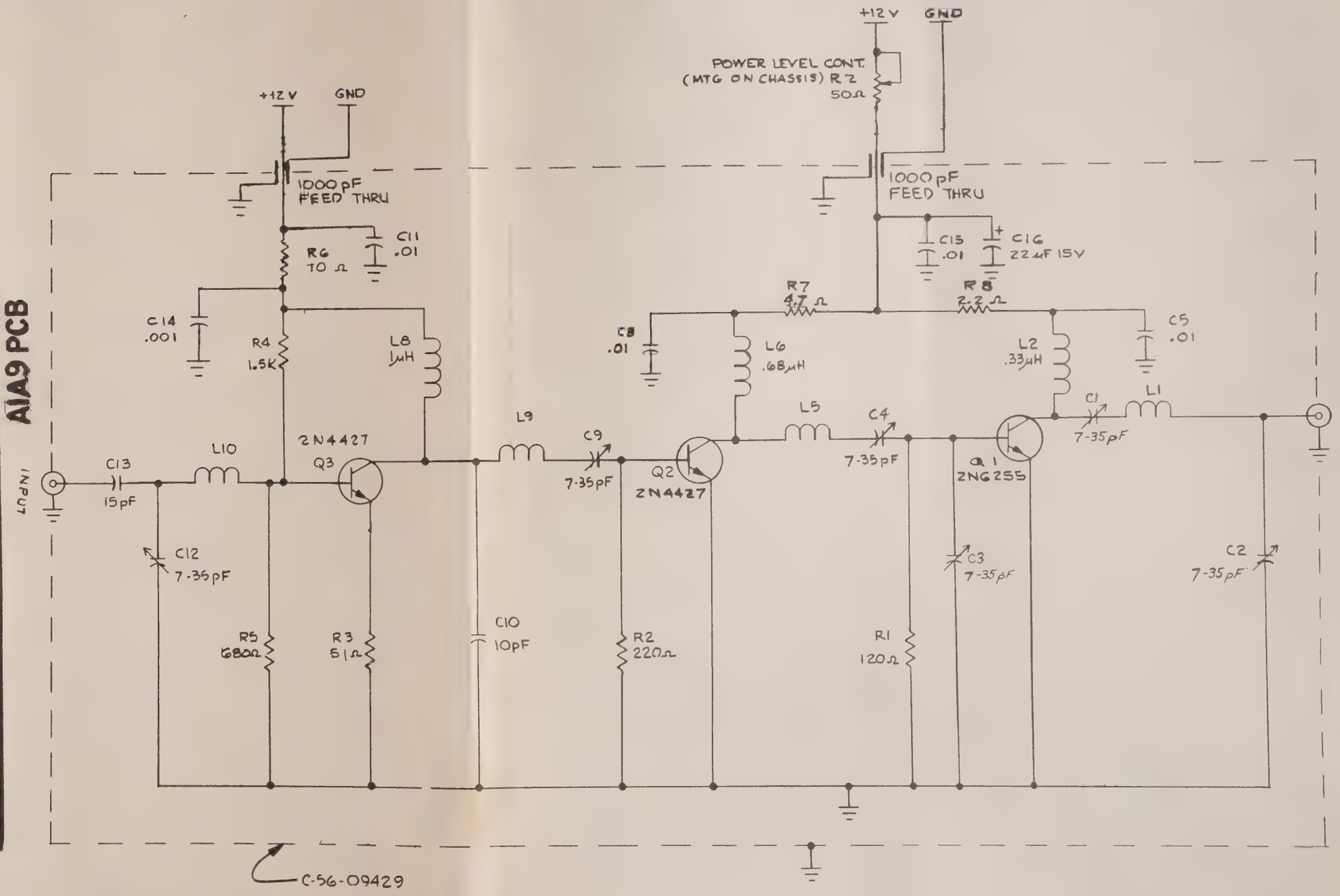
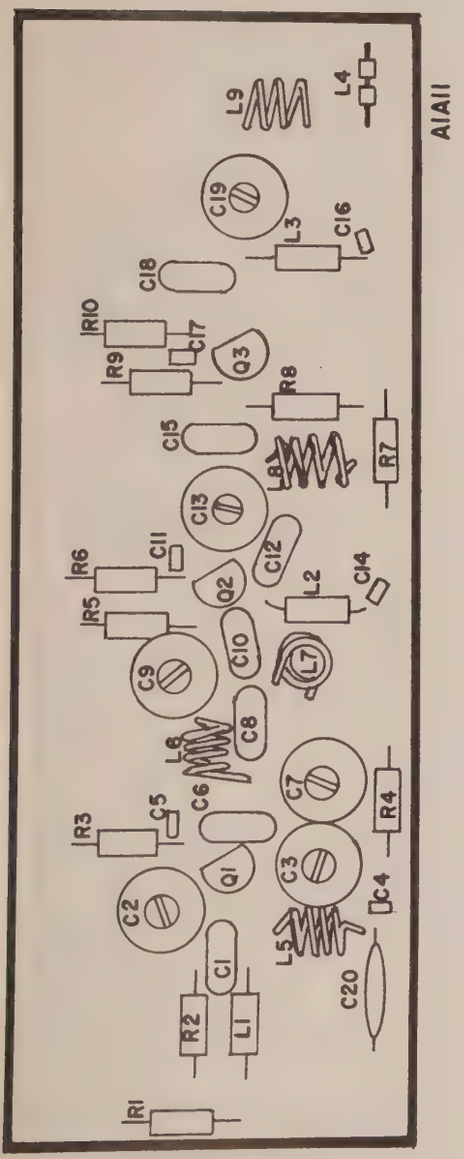


FIGURE 6-13
200 MHZ POWER AMPLIFIER ASSEMBLY (A1A9), SCHEMATIC AND COMPONENT LOCATION DIAGRAM
(C-11-09447)



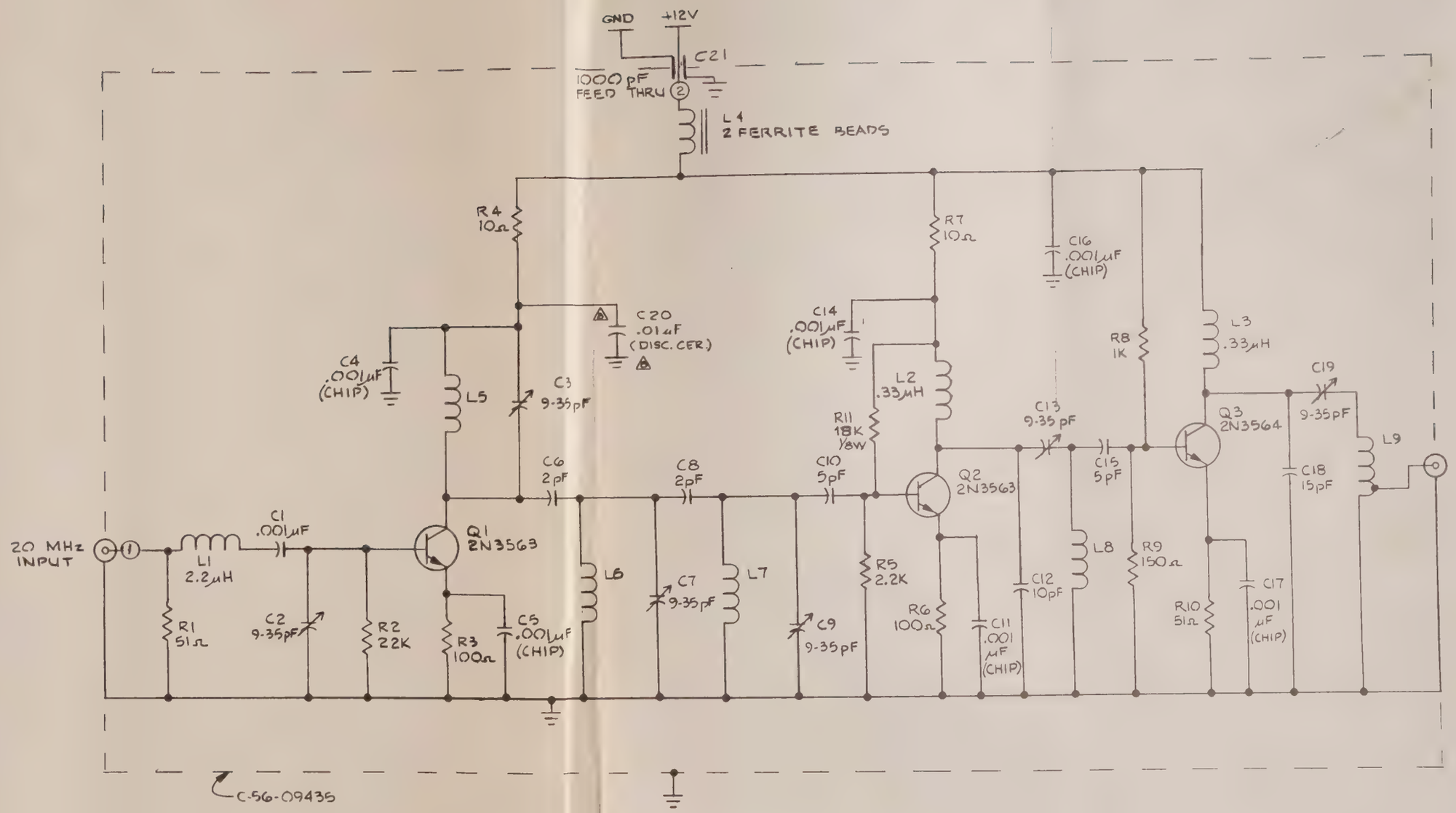
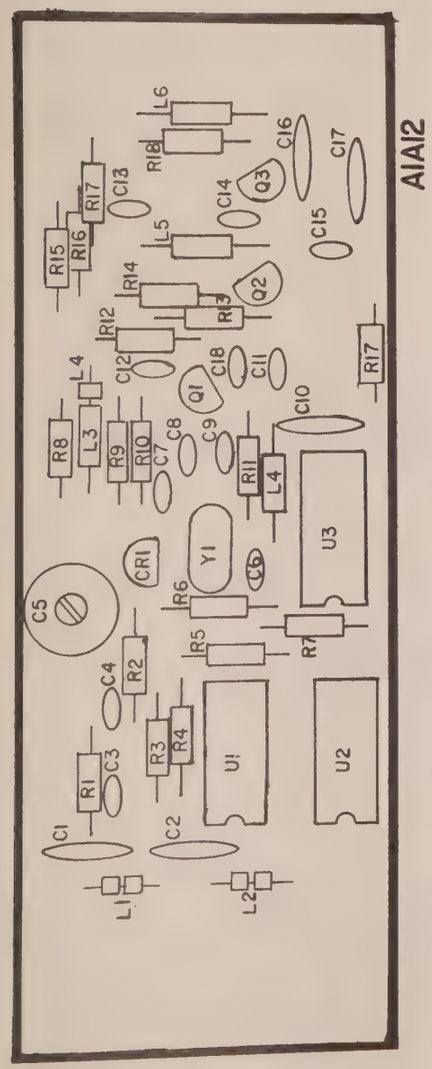
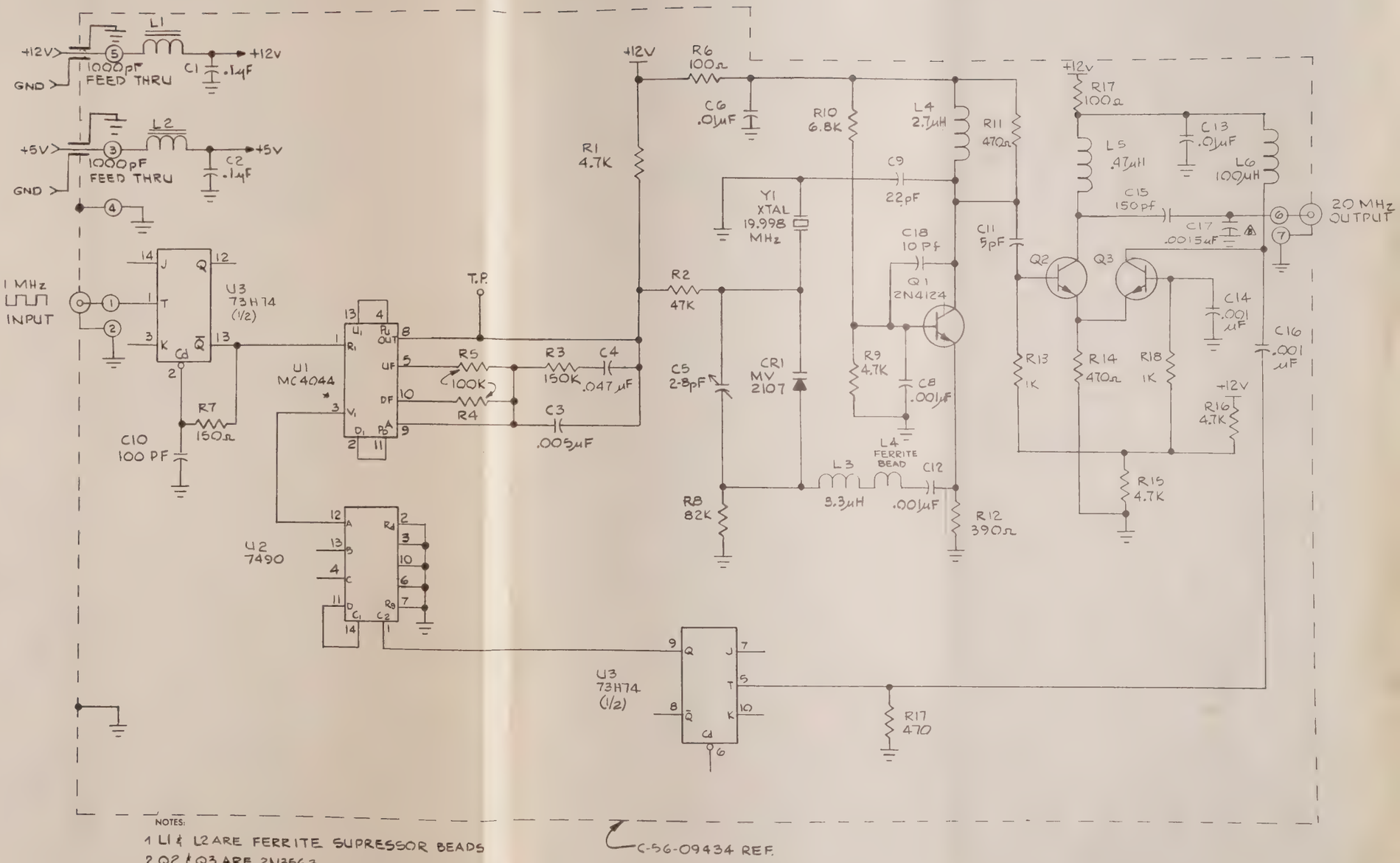


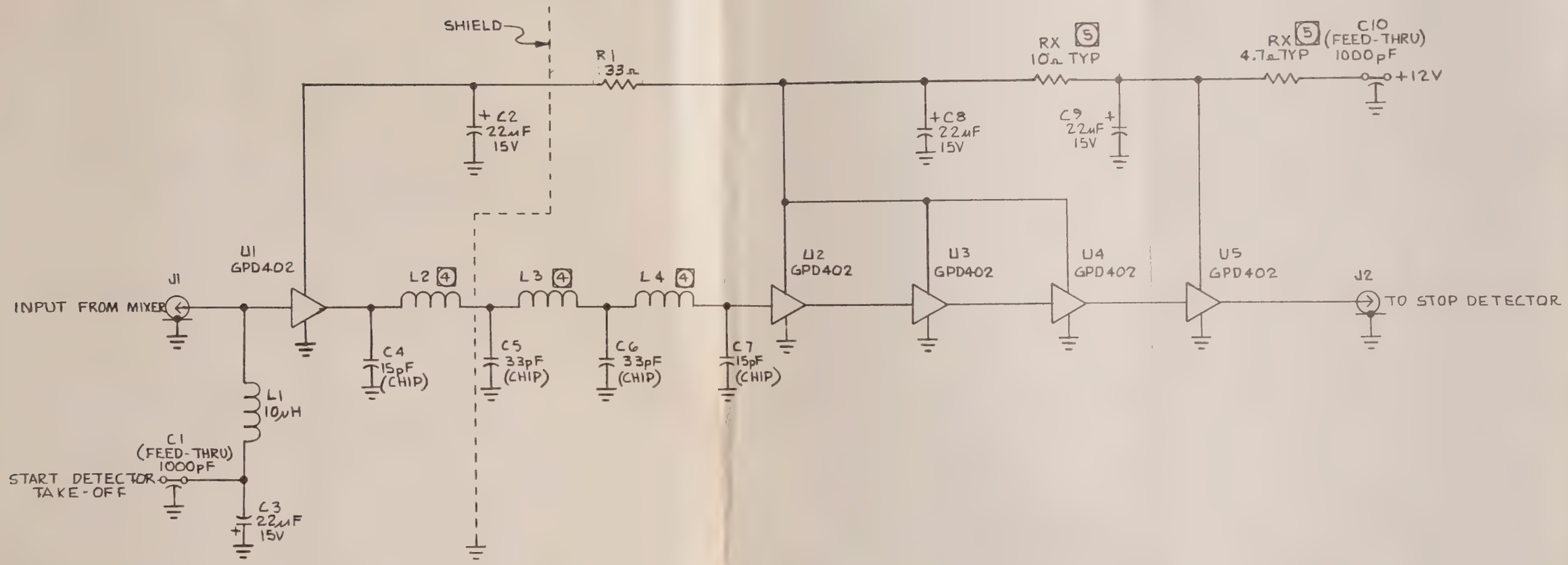
FIGURE 6-14
200 MHZ FREQUENCY MULTIPLIER ASSEMBLY (A1A11), SCHEMATIC AND COMPONENT LOCATION DIAGRAM (C-11-09469)

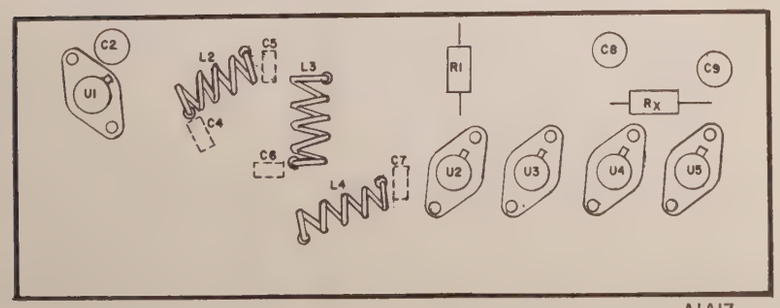




NOTES:
1 L1 & L2 ARE FERRITE SUPRESSOR BEADS
2 Q2 & Q3 ARE 2N3563
3 ADJUST C5 FOR 8V AT T.P.
4 ADJUST L FOR MAX 20 MHz OUTPUT INTO 50Ω.
5. ALL RESISTORS - ALLEN BRADLEY TYPE CARBON COMP.
6. P.C. ASSY 09451

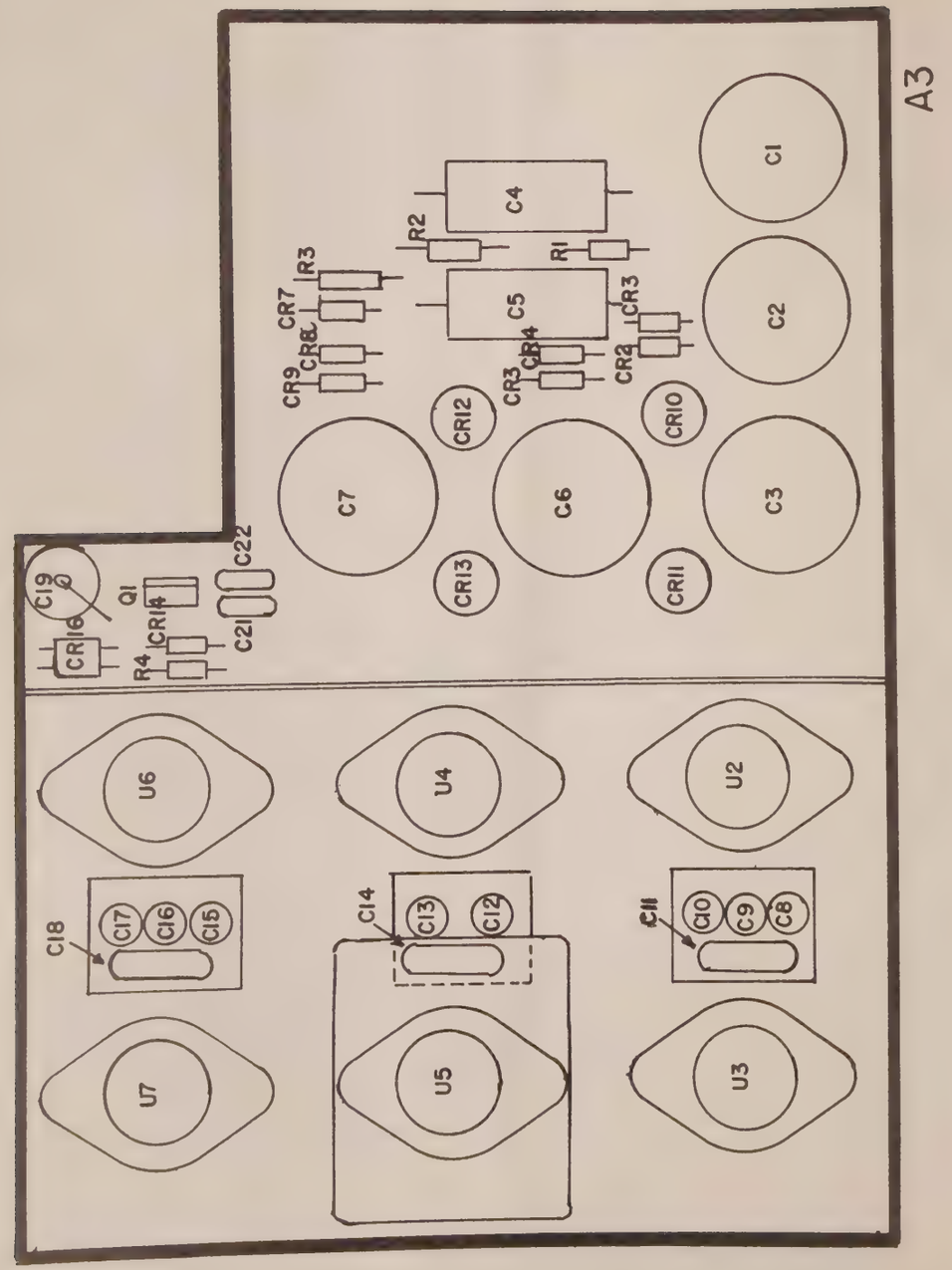
FIGURE 6-15
20 MHZ PHASE LOCK OSCILLATOR ASSEMBLY (A1A12), SCHEMATIC AND COMPONENT LOCATION DIAGRAM (C-11-09450)





A1A13

FIGURE 6-16
IF AMPLIFIER ASSEMBLY (A1A13),
SCHEMATIC AND COMPONENT
LOCATION DIAGRAM
(C-11-11182)



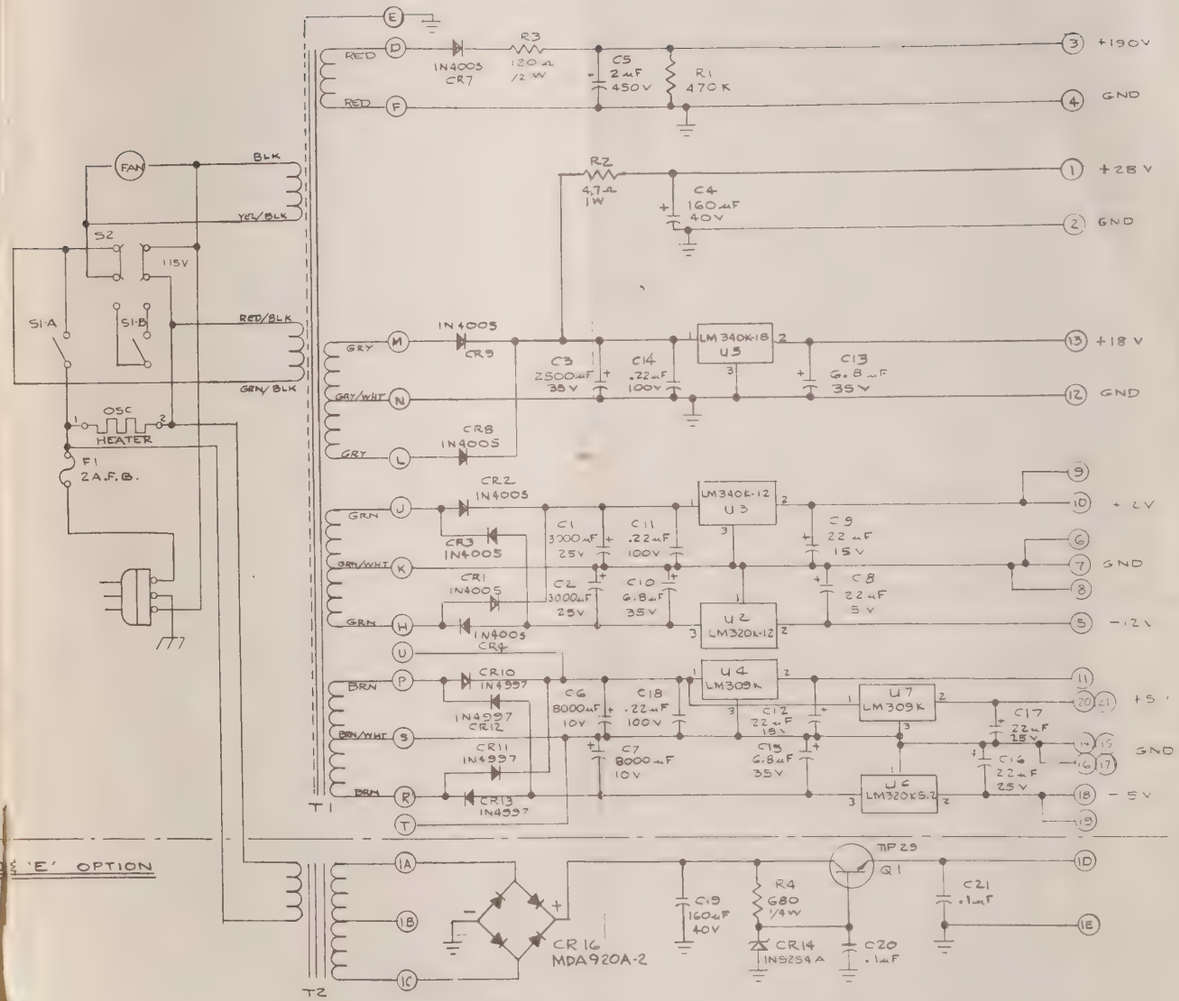


FIGURE 6-17
POWER SUPPLY ASSEMBLY (A3), SCHEMATIC AND COMPONENT LOCATION DIAGRAM

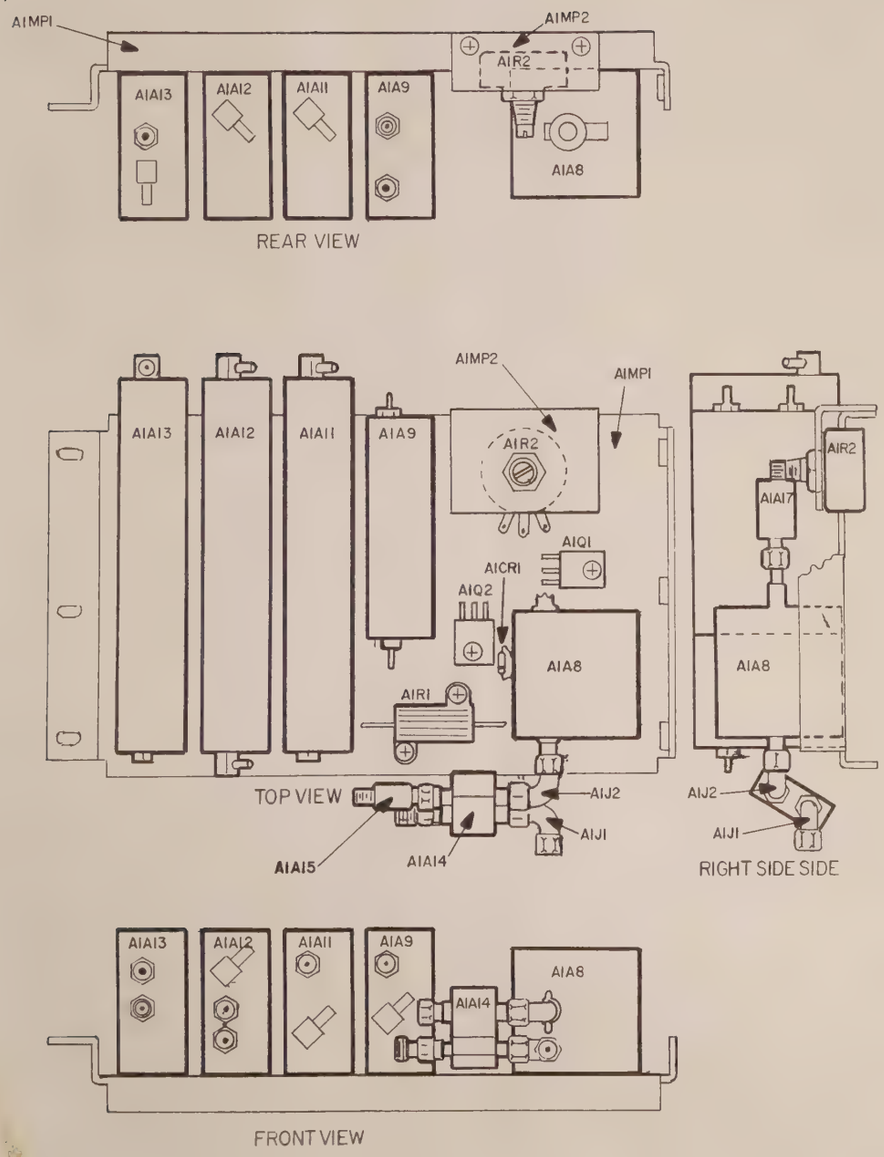
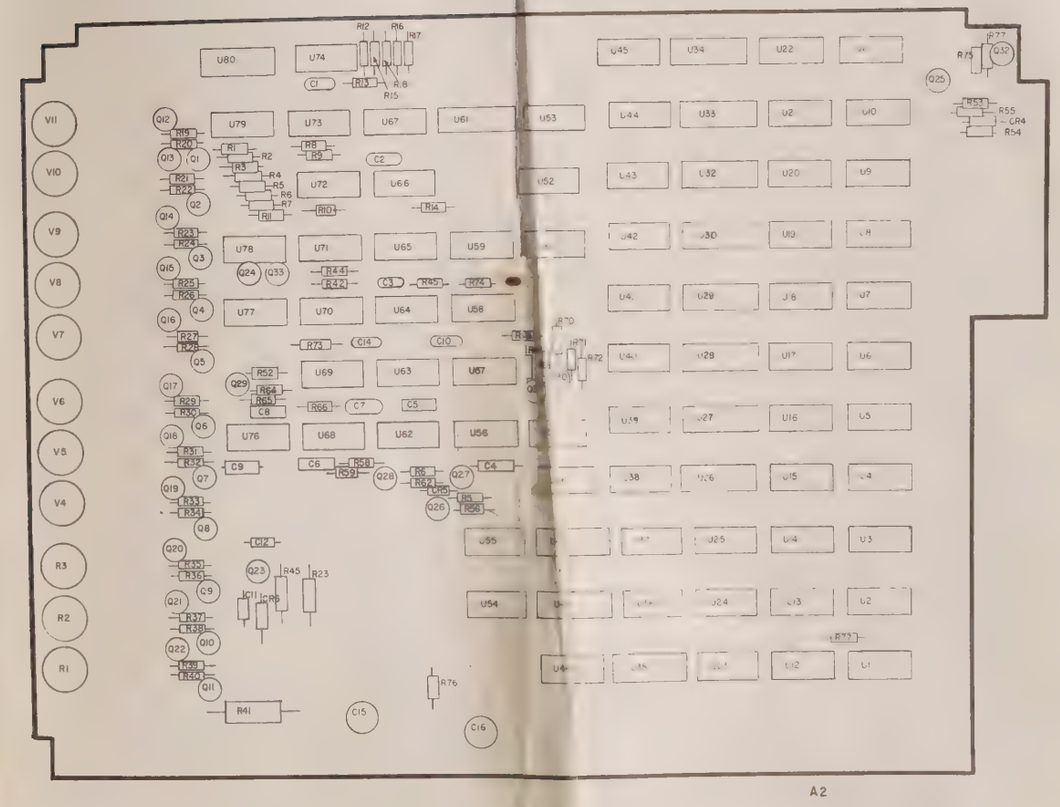


FIGURE 6-18
AUTO HET ASSEMBLY (A1),
COMPONENT LOCATION DIAGRAM



URE 6-19
OUNTER/DISPLAY PCB ASSEMBLY
(A2), COMPONENT LOCATION DIAGRAM

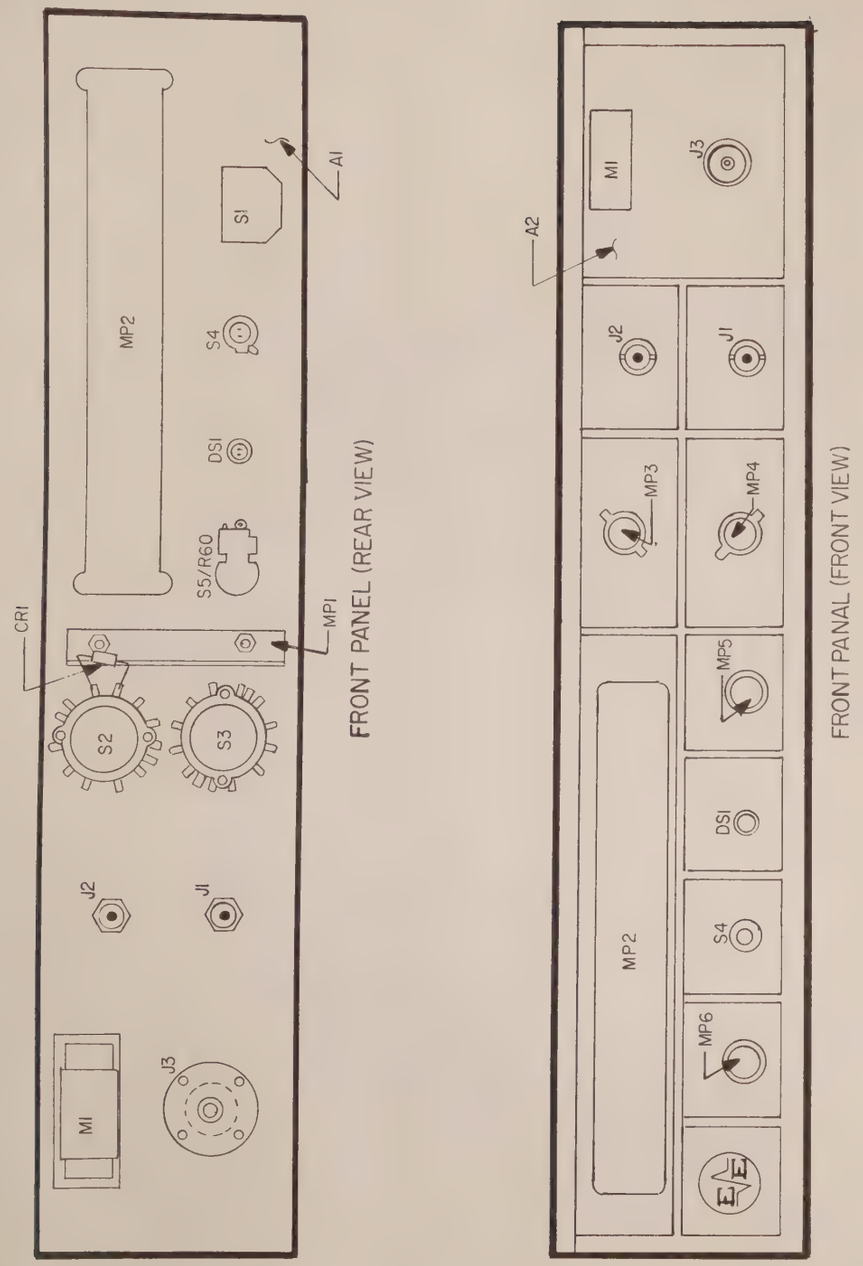


FIGURE 6-20
FRONT PANEL ASSEMBLY (A4),
COMPONENT LOCATION DIAGRAM

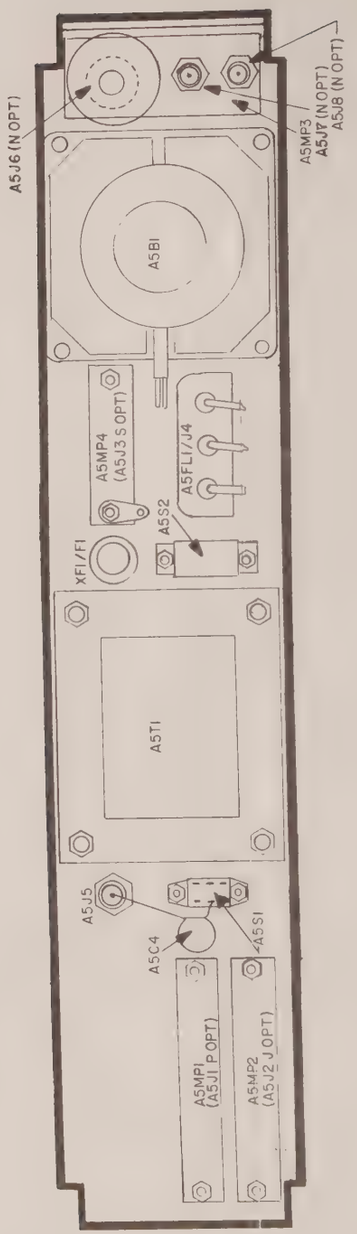


FIGURE 6-21
REAR PANEL ASSEMBLY (A5),
COMPONENT LOCATION DIAGRAM

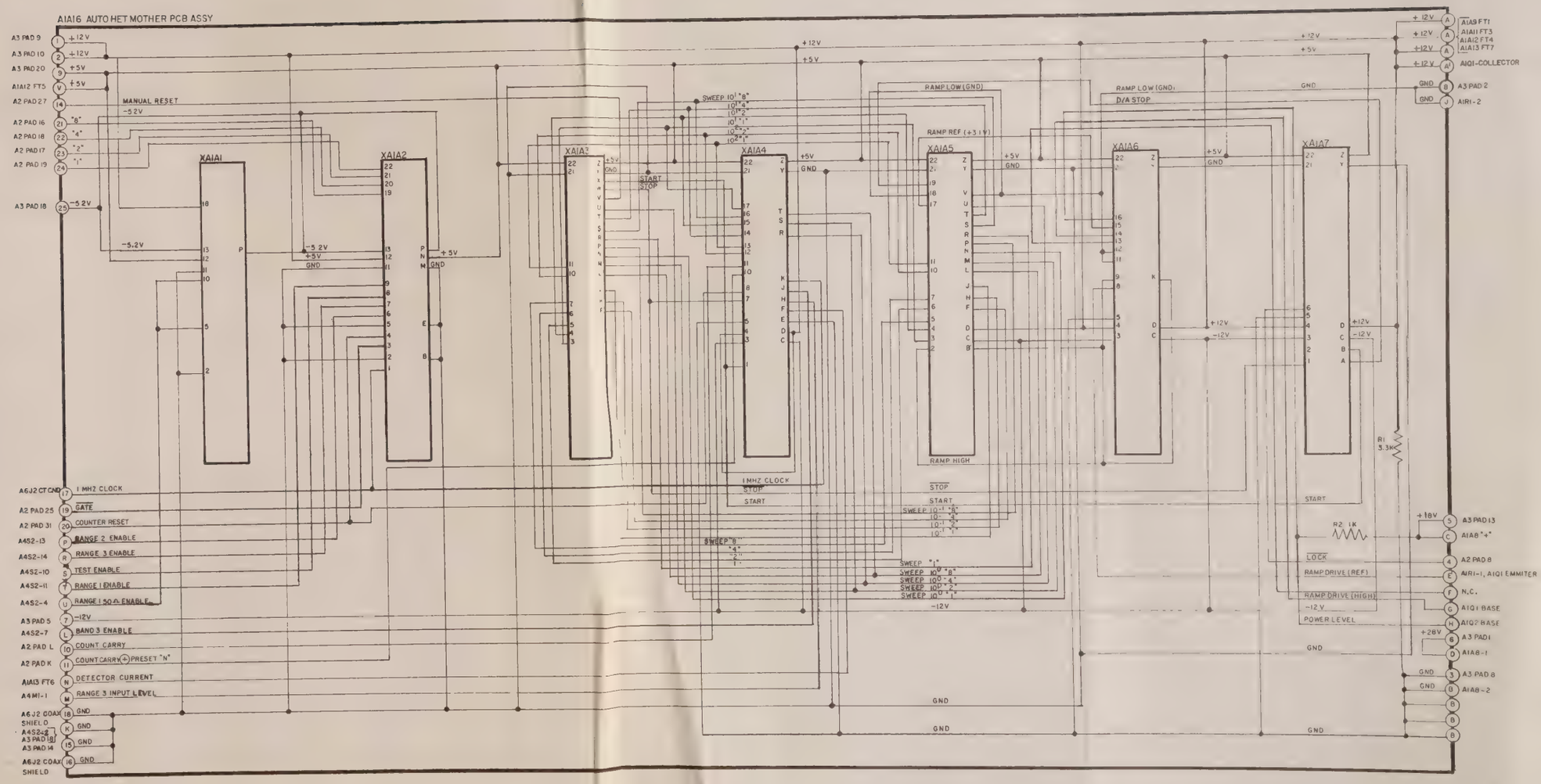
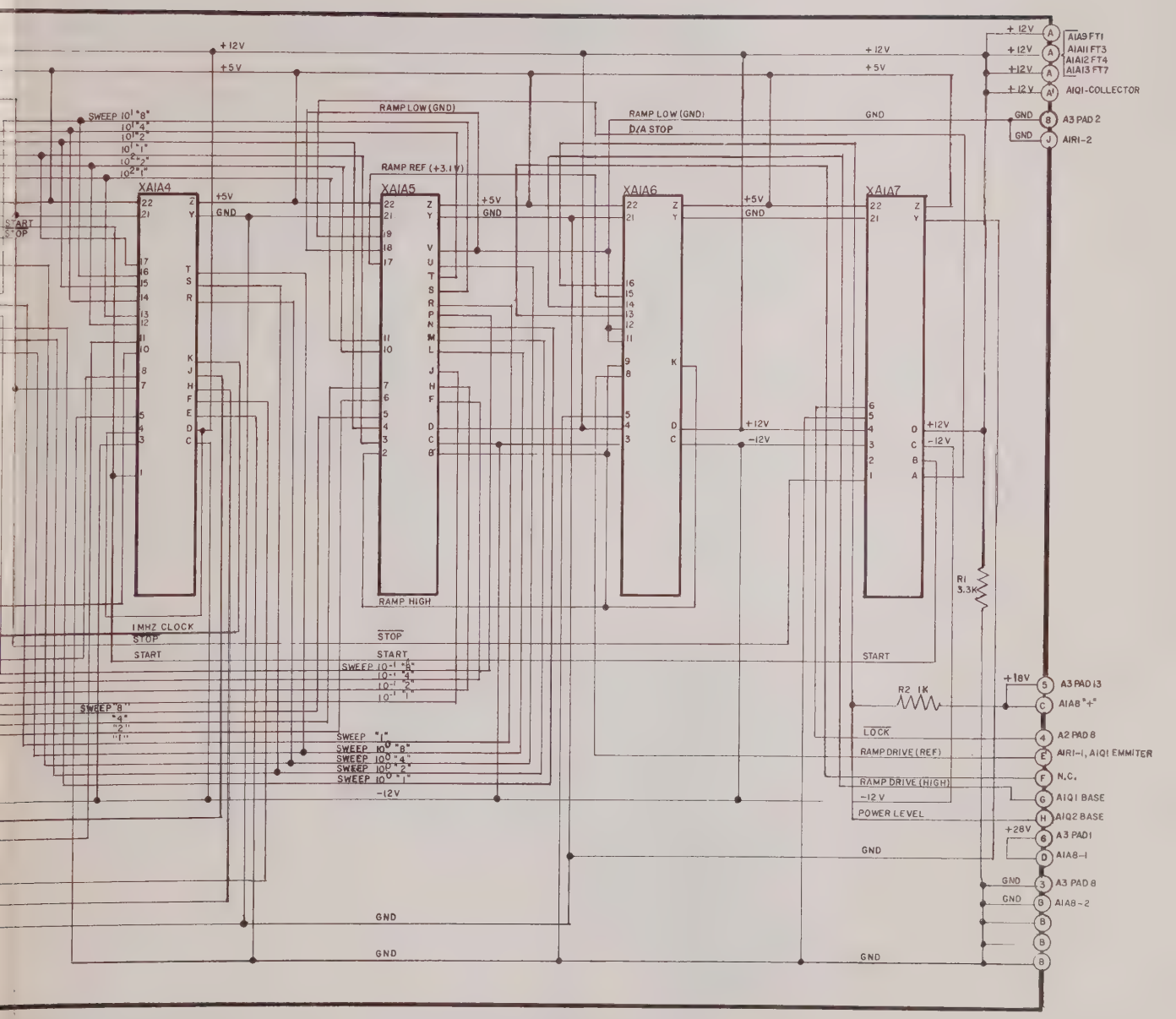


FIGURE 6-22
AUTO HET INTERCONNECT
SCHEMATIC DIAGRAM
(D-11-11267)


+12V
+5V
GND
XA1A4
XA1A5
XA1A6
XA1A7
RAMP LOW (GND)
RAMP REF (+3.1V)
D/A STOP
RAMP HIGH
1MHZ CLOCK
STOP
START
SWEEP "8"
"4"
"2"
"1"
-12V
R1 3.3K
R2 1K
LOCK
RAMP DRIVE (REF)
RAMP DRIVE (HIGH)
POWER LEVEL
+28V
+18V
A1A9 FT1
A1A11 FT3
A1A12 FT4
A1A13 FT7
A1Q1-COLLECTOR
A3 PAD 2
A1R1-2
A3 PAD 13
A1A8 "+"
A2 PAD 8
A1R1-1, A1Q1 EMMITER
N.C.
A1Q1 BASE
A1Q2 BASE
A3 PAD 1
A1A8-1
A3 PAD 8
A1A8-2

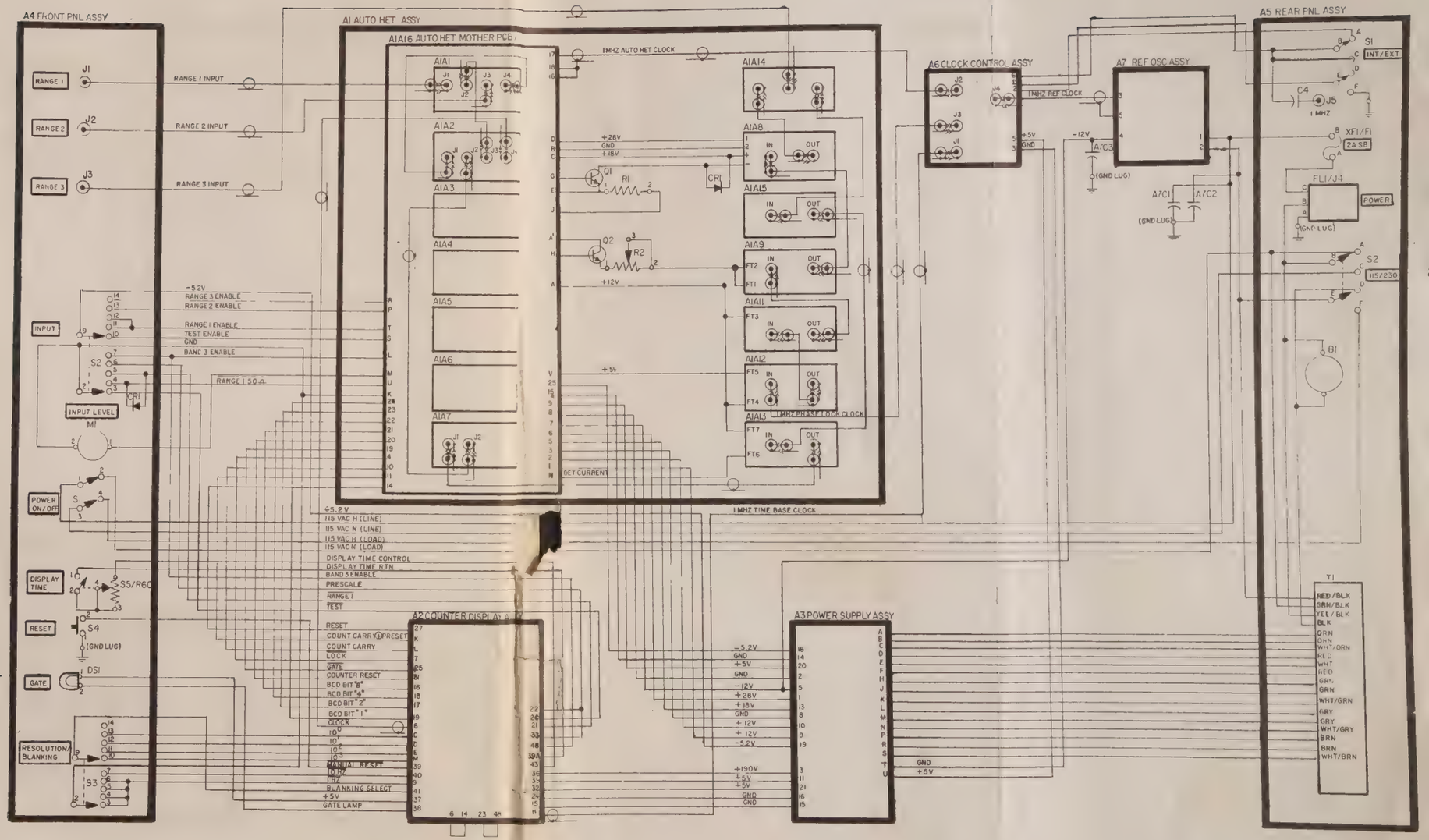
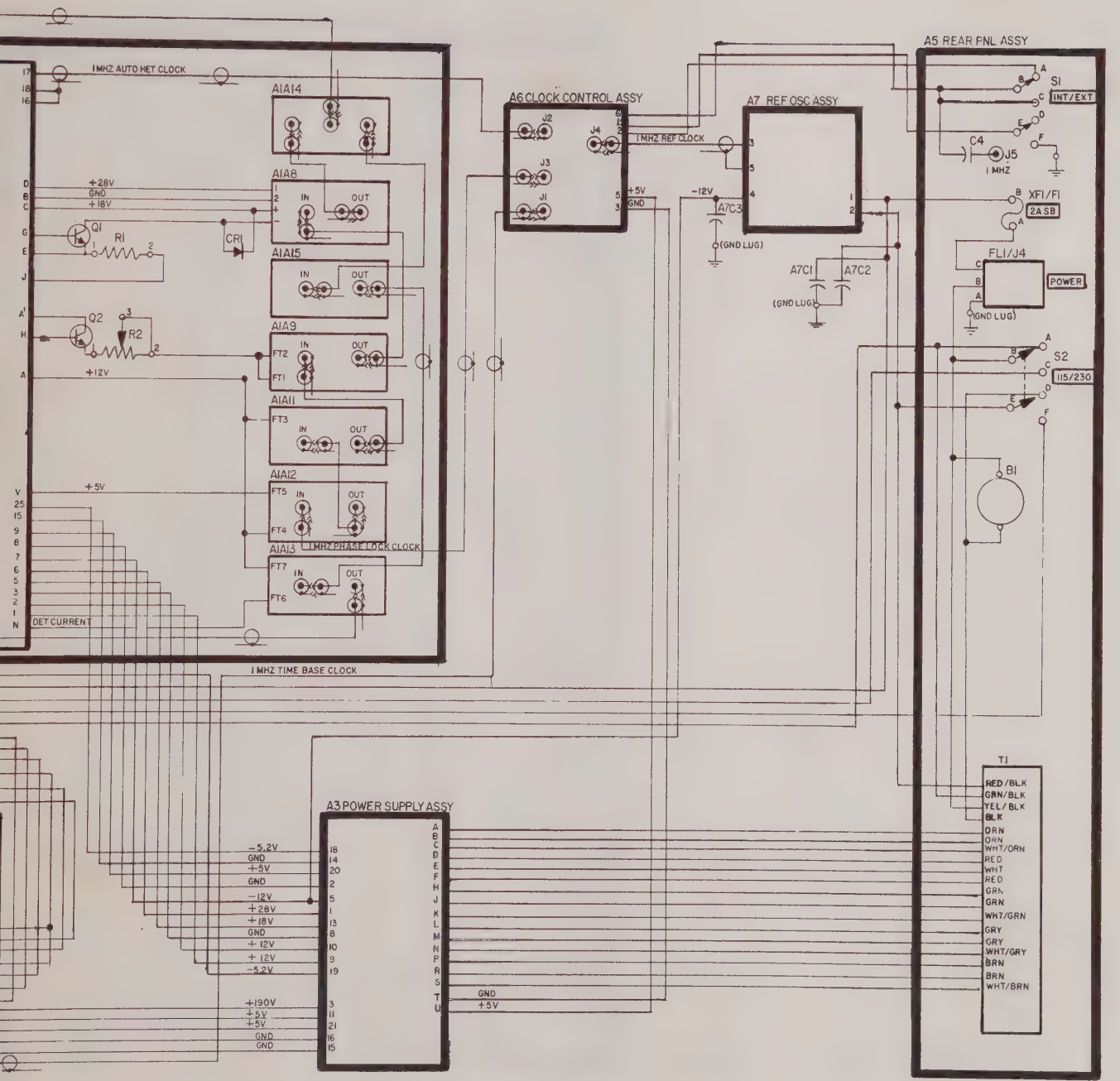


FIGURE 6-23
INTERCONNECT SCHEMATIC DIAGRAM
(D-11-10735)


A5 REAR PNL ASSY
A6 CLOCK CONTROL ASSY
A7 REF OSC ASSY
A3 POWER SUPPLY ASSY
1MHZ AUTO HET CLOCK
1MHZ REF CLOCK
1MHZ PHASE LOCK CLOCK
1MHZ TIME BASE CLOCK
DET CURRENT
A1A14
A1A8
A1A15
A1A9
A1A11
A1A12
A1A13
+28V
GND
+18V
+12V
+5V
-12V
Q1
Q2
R1
R2
CR1
A7C1
A7C2
A7C3
(GND LUG)
S1
INT/EXT
S2
115/230
C4
J5
1 MHZ
XF1/F1
2A SB
FL1/J4
POWER
B1
T1
RED/BLK
GRN/BLK
YEL/BLK
BLK
ORN
ORN
WHT/ORN
RED
WHT
RED
GRN
GRN
WHT/GRN
GRY
GRY
WHT/GRY
BRN
BRN
WHT/BRN
-5.2V
+190V

SECTION 7

MODEL 988/989 OPTIONS

SECTION 7
MODEL 988/989 OPTIONS

7.1 INTRODUCTION

This section describes the available options that may be incorporated into the basic Model 988/989 Microwave Frequency Counter. On the serialized nomenclature plate located on the rear panel of the instrument is the model number, option (s) and special modification legend data in the following format.

Table 7-1 lists and provides a brief description of the options that are available with the Model 988/989 Microwave Frequency Counter.

TABLE 7-1 MODEL 988/989 OPTIONS

C1	A internal temperature controlled crystal oscillator assembly with the same stability as the standard oscillator, but for 230 Vac operation only.
D	A internal temperature controlled 5 MHz crystal oscillator assembly with increased stability over the standard oscillator assembly having the following specifications. Short Term Stability: 5×10^{-10} per 7 minutes. Long Term Stability: 2×10^{-9} per day, after 48 hours warm up. Temperature Stability: 2×10^{-10} per °C (average) from 0°C to +50°C. Retracability: $\pm 5 \times 10^{-10}$ of the previous frequency after 60 minutes operation following a 24 hour off period.
D1	A internal temperature controlled 5 MHz crystal oscillator assembly as in option D but with a power supply configured for 230 Vac line operation.
E	A internal temperature controlled 5 MHz crystal oscillator assembly with increased stability over the standard oscillator assembly having the following specifications. Short Term Stability: 5×10^{-10} per 7 minutes. Long Term Stability: 1×10^{-9} per day, after 48 hours warm up. Temperature Stability: 2×10^{-10} per °C (average) from 0°C to +50°C. Retracability: $\pm 5 \times 10^{-9}$ of the previous frequency after 1 hour operation following a 24 hour off period.

TABLE 7-1 MODEL 988/989 OPTIONS
(Continued)

E1	A internal temperature controlled 5 MHz crystal oscillator assembly as in option E but with a power supply configured for 230 Vac line operation.
F	Provides wiring and logic to allow remote preseting of the counter to any desired number from all zeros to 1999999000 in 1 KHz increments. The preset number is determined by a 32 line BCD input via a optional rear panel 50 pin Amphenol 57-40500 connector. This option is provided to allow receiver local oscillator monitoring and similar measurement applications.
G	A internal temperature controlled 5 MHz crystal oscillator assembly with increased stability of the standard reference oscillator having the following specifications. Short Term Stability: 5×10^{-11} per 1 second average. Long Term Stability: 5×10^{-10} per day, after 72 hours operation. Temperature Stability: 2×10^{-10} per °C (average) from 0°C to +5°C. Retracability: $\pm 5 \times 10^{-9}$ of the previous frequency after 1 hour operation following a 24 hour off period.
G1	A internal temperature controlled crystal oscillator as in option G but with a power supply configured for 230 Vac line operation.
J	Provides wiring for the remote selection of Range 1, 2, 3 and Test function via a optional rear panel connector by remote contact closures or saturated NPN transistors to ground. Also provides remote control of the Display Time by a 1 MΩ external variable resistor.
L	Provides the additional components for the Range 2 function; 25 MHz to 625 MHz with a 100 mV rms input sensitivity utilizing a prescaler to divide the signal by 4.
N	Relocation of the Input RF connectors to the instruments rear panel to allow the Frequency Counter to be intergrated into a systems configuration.
P	Provides for BCD measurement data output via 44 lines to a rear panel mounted 50 pin Amphenol 57-40500 connector. The output data is positive zone true logic in 1-2-4-8 BCD format where "1" = 5V and "0" = 0V nominal.
R5	Provides rack mounting hardware to allow the instrument to be mounted in a standard 19 inch relay rack for systems intergration.
S	Provides for the remote selection of the Auto Het (YIG) sweep start and stop frequency three most significant digits via a 18 line BCD format inputed thru a rear panel 24 pin Amphenol 57-40240 connector. This option allows the Range 3 frequency range to be limited as to its start and stop (lower and upper) frequency remotely for special systems applications.

TABLE 7-1 MODEL 988/989 OPTIONS
(Continued)

T	Provides for switch selection of 115 or 230 Vac line operation, and 50 to 400 Hz line frequency for Fan operation.

7.2 OPTION C1

Option C1 differs from the standard Model 988/989 Counter in that the Reference Oscillator Assembly (A7) is replaced with a Reference Oscillator having a 230 Vac heater element, (Monitor part number S0-3047), the addition of 3 filter capacitors and wiring modification to allow 230 Vac interconnection. Figure 7-1 provides an interconnect diagram illustrating the Option C1 component and wiring configuration.

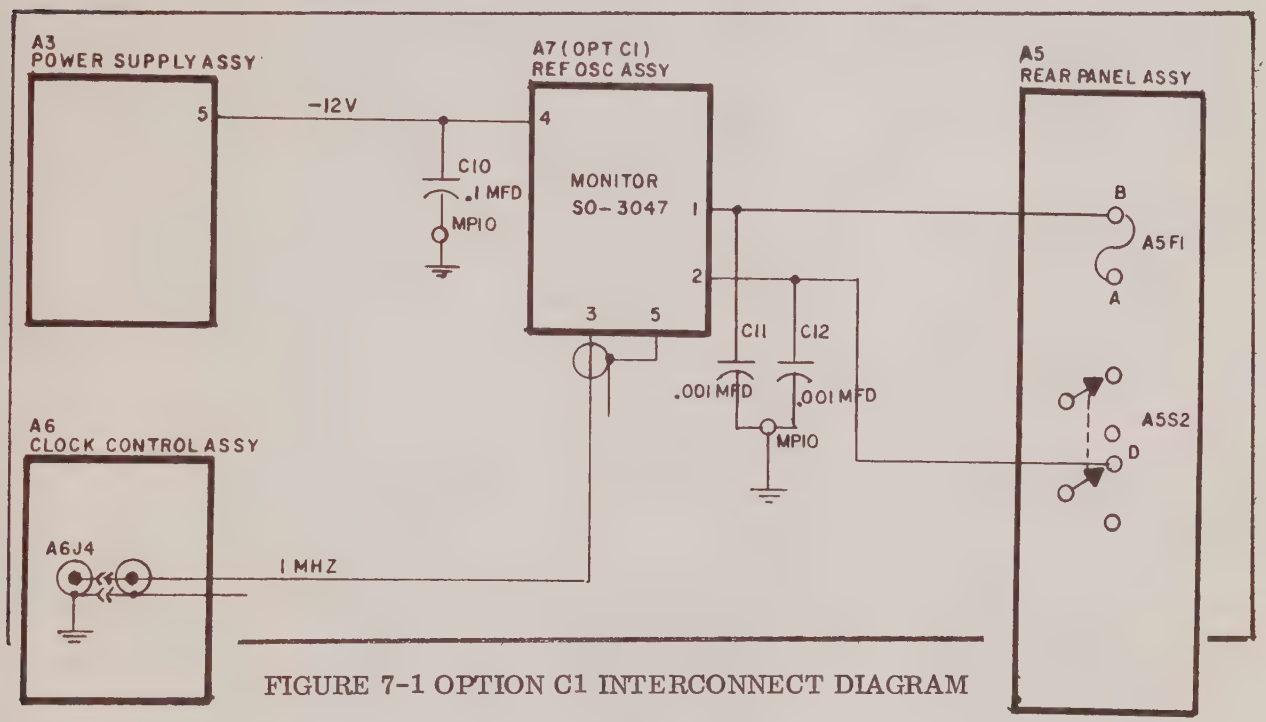


FIGURE 7-1 OPTION C1 INTERCONNECT DIAGRAM

A parts list is provided that lists the Option C1 Oscillator Assembly and the added components required for the Option C1 incorporation.

Reference	Description	Mfg.	Mfg. No.	EI No.	Qty.
A7 (C1)	Oscillator Assembly 1 MHz, (Option C1)	MONITOR	SO-3047	003345	1
C10	Capacitor, 0.1μF, 250 WVDC, Mylar	AMPE	C28AE/P100K	000211	1
C11, 12	Capacitor, .001μF, 100WVDC	CRL	DD-120	000117	2
MP10, 11	Lug, Ground, #4	EI		003876	2

7.3 OPTION D AND D1

Option D and D1 provides a Reference Oscillator Assembly A7 (D, D1) that has a greater stability than the standard reference oscillator A7. The optional D and D1 reference oscillator is a Austron 1100-2, which utilizes a 26 V dc internal oven (heater element), and when configured into the standard Model 988/989 Counter, a power transformer T2 (D, D1) and a +26V power supply/regulator is incorporated. Refer to Figure 6-17 Power Supply Assembly (A3 Schematic Diagram located on page 6-37 of this manual for the optional power supply configuration. The optional D and D1 reference oscillator outputs a 5 MHz signal, and a IC type SN7490 (A6U2) is added to the Clock Control PCB Assembly (A6) to provide a ÷ 5 count down to generate the required 1 MHz reference clock. Refer to Figure 6-2 Clock Control Schematic Diagram, located on page 6-7 of this manual for the ÷ 5 counter (A6U2) circuit relationship. Figure 7-2 provides an interconnect diagram that illustrates the component and wiring configuration of the D and D1 options.

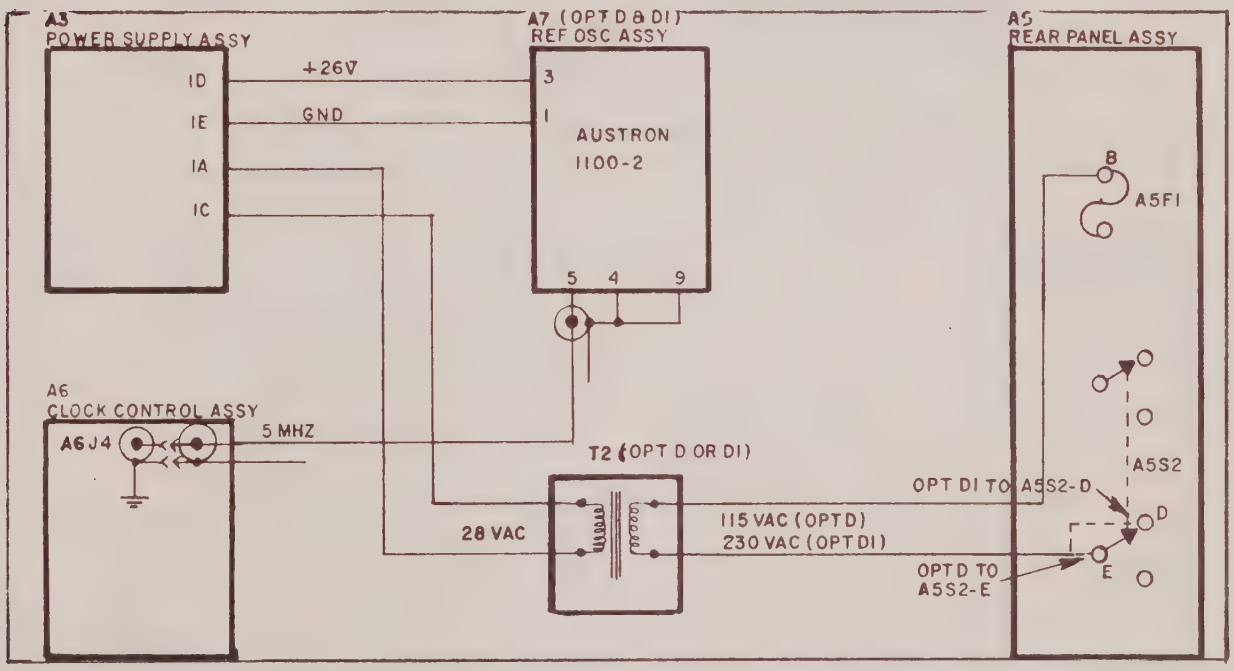


FIGURE 7-2 OPTION D AND D1 INTERCONNECT DIAGRAM

The parts list provided below lists the optional D and D1 reference Oscillator Assembly and the additional components required to configurate the option.

OPTION D, D1 PARTS LIST

Reference	Description	Mfg.	Mfg. No.	EI No.	Qty.
A3 (D, E)	Power Supply Assy, (Modified D and E Options)	EI	A-11213		1

OPTION D, D1 PARTS LIST
(Continued)

Reference	Description	Mfg.	Mfg. No.	EI No.	Qty.
A6U2	Intergrated Circuit, Type SN7940	TI	SN7490	004729	1
A7 (D, D1)	Oscillator Assembly, 5 MHz (Option D and D1)	AUSTRON	1100-2	003119	1
T2 (D)	Transformer, Power, 115 Vac Pri., 28 Vac Sec, (Option D)	STANCOR	P3895	003679	1
T2 (D1)	Transformer, Power, 230 Vac Pri, 28 Vac Sec, (Option D1)	STANCOR		003662	1
XA7	Socket, Assy., 9 pin	EI		003492	1

7.4 OPTION E AND E1

Option E and E1 provides a reference Oscillator A7 (E, E1) that has a greater stability than the standard reference oscillator A7. The optional E and E1 reference oscillator is an Austron 1100-1, which utilizes a 26 V dc internal oven (heater element), and when configured into the standard Model 988/989 Counter a power transformer T2 (E, E1) and a +26V power supply/regulator is incorporated. Refer to Figure 6-17 Power Supply Assembly (A3 Schematic Diagram located on page 6-37 of this manual for the optional power supply configuration. The optional E and E1 reference oscillator outputs a 5 MHz signal, and a IC type SN7490 (A6U2) is added to the Clock Control PCB Assembly (A6) to provide ÷ 5 count down to generate the required 1 MHz reference clock. Refer to Figure 6-2 on page 6-7 of this manual for the ÷ 5 counter (A6U2) circuit relationship. Figure 7-3 provides an interconnect diagram that illustrates the component and wiring configuration of the E and E1 options.

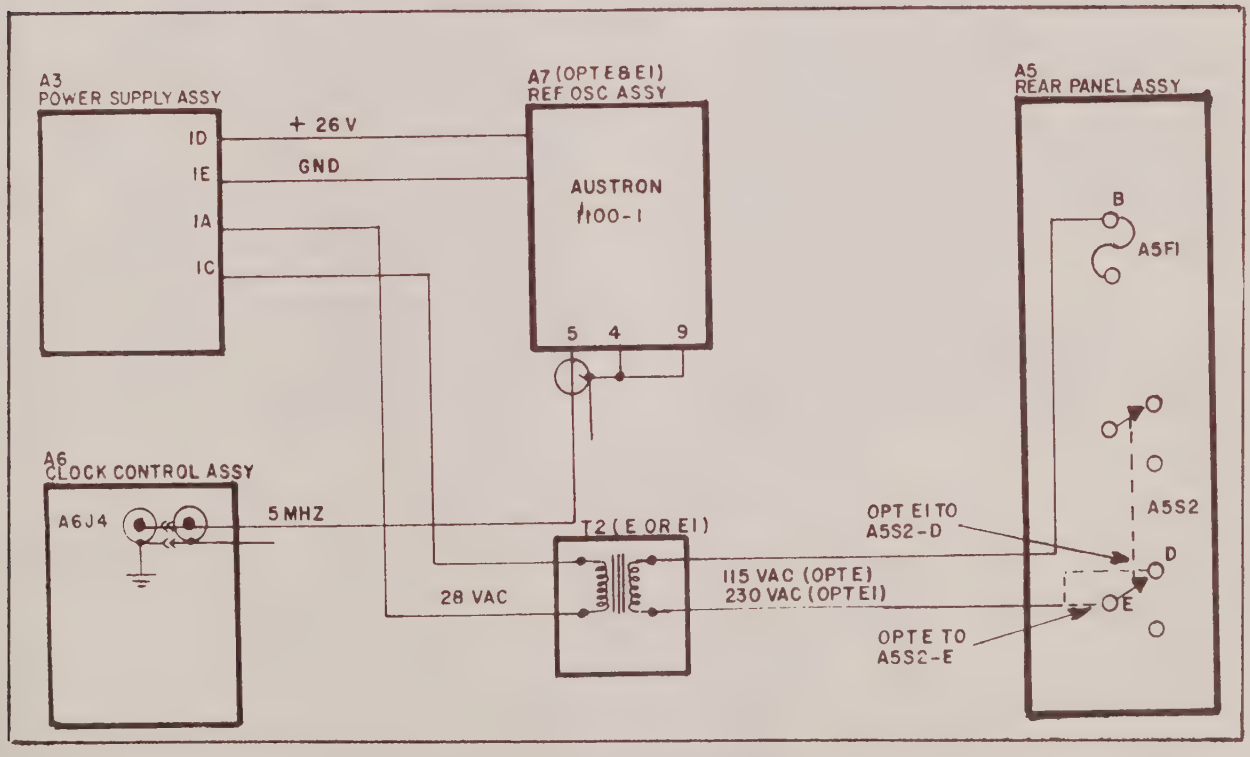


FIGURE 7-3 OPTION E AND E1 INTERCONNECT DIAGRAM

The following parts list provides ordering information on the optional E and E1 Reference Oscillator Assembly and the additional components required to configurate the option.

OPTION E AND E1 PARTS LIST

Reference	Description	Mfg.	Mfg. No.	EI No.	Qty.
A3 (D, E)	Power Supply Assy. (Modified D and E Options.)	EI	A-11213		1
A6U2	Intergrated Circuit Type SN7490	TI	SN7490	004729	1
A7 (E, E1)	Oscillator Assembly 5 MHz (Option E, E1)	AUSTRON	1100-1	003509	1
T2 (E1)	Transformer, Power 115 Vac Pri, 28 Vac Sec.	STACOR	P-8395	003679	1
T2 (E1)	Transformer, Power 230 Vac Pri, 28 Vac Sec.	STACOR		003662	1
XA7	Socket, Assy., 9 pin	EI		003492	1

7.5 OPTION F

Option F provides for the remote preseting of the counters 10^3 thru 10^{10} DCU's via a BCD 38 line rear panel connector input, which allows the counter to be preset to any desired decimal number from all zeros to 1999999000. This optional feature will allow receiver local oscillator frequency monitoring and similar measurement applications that require a preset-offset of the count chain.

The 10^3 thru 10^{10} DCU's (A2U15 thru U2U22) are 50 MHz Presettable DCU/ Latches IC Type SN74196. Preset/Reset control logic consisting of U58D and E inverters and U57A and B NAND gates is configured into the standard instrument. The following circuit analysis of the Option F logic contained in the standard instrument configuration is referenced to figure 6-4 Count Chain Schematic Diagram sheets 1 and 2. A PRESET ENABLE command siganl from the remote device is applied to U57A at pin 2 via PCB pad A2-10 where it is NAND gated with RESET signal applied to pin 1 via inverter U58E. The NAND gate U57A outputs at pin 3 the ENTER command which is wired to pin 1 of the 10^3 thru 10^{10} DCU's (U15 thru U22). When the ENTER command is at a logic low the 1-2-4-8 BCD data presented on pins 4, 10, 3 and 11 of the DCU's is entered, thus presetting the counter. The type SN74196 IC's are cleared (reset to zero) as a direct logic low function, and the preset enable (ENTER) is also a direct logic low function. To prevent logical confliction between the reset and the preset enable functions, the inverter/NAND gate configuration consisting of U58D and E and U57A and B will inhibit the generation of an ENTER command when a RESET signal is inputed. And in its complementry function will inhibit the generation of a RESET command when a PRESET ENABLE is entered.

The 10^3 is the least significant digit that can be preset and represents the 1 KHz column of the counters visual display. All the decades from 10^3 thru 10^9 can be preset to any decimal number from 0 to 9. The 10^{10} digit is the most significant digit that can be preset and represents the 10 GHz column of the visual display, this decade can be preset to a decimal number of only 0, 1, 8 or 9 (BCD Bits "1" and/or "8").

The Option F is physically configured by installing a 50 pin Amphenol 57-40500 connector (A5J2) on the instruments rear panel and hard wiring its connector pins to the appropriate pads on the Counter PCB Assembly (A2). This rear panel optional connector is also used for the Option J configuration. When and if Option J is installed refer to paragraph 7.7 for the required wiring data.

The following wire list provides the interconnect interface data of the rear panel Option F connector pins to the PCB Assembly A2 pads.

OPTION F INTERFACE WIRE LIST

A5J2 PIN NO.	SIGNAL NAME	A2 PAD NO.
1	10^3 Bit "1" PRESET	75
2	10^3 Bit "2" PRESET	91
3	10^4 Bit "1" PRESET	73
4	10^4 Bit "2" PRESET	89
5	10^5 Bit "1" PRESET	71
6	10^5 Bit "2" PRESET	87
7	10^6 Bit "1" PRESET	69

OPTION F INTERFACE WIRE LIST (Cont'd)

A5J2 PIN NO.	SIGNAL NAME	A2 PAD NO.
8	10^6 Bit "2" PRESET	85
9	10^7 Bit "1" PRESET	67
10	10^7 Bit "2" PRESET	83
11	10^8 Bit "1" PRESET	65
12	10^8 Bit "2" PRESET	81
13	10^9 Bit "1" PRESET	63
14	10^9 Bit "2" PRESET	79
15	10^{10} Bit "1" PRESET	61
16	OPTION J INTERFACE	
17	OPTION J INTERFACE	
18	OPTION J INTERFACE	
19	OPTION J INTERFACE	
20	OPTION J INTERFACE	
21	OPTION J INTERFACE	
22	OPTION J INTERFACE	
23	OPTION J INTERFACE	
24	OPTION J INTERFACE	
25	+5 VOLT LOGIC HIGH REF	92
26	10^3 Bit "4" PRESET	74
27	10^3 Bit "8" PRESET	90
28	10^4 Bit "4" PRESET	72
29	10^4 Bit "8" PRESET	88
30	10^5 Bit "4" PRESET	70
31	10^5 Bit "8" PRESET	86
32	10^6 Bit "4" PRESET	68
33	10^6 Bit "8" PRESET	84
34	10^7 Bit "4" PRESET	66
35	10^7 Bit "8" PRESET	82
36	10^8 Bit "4" PRESET	64
37	10^8 Bit "8" PRESET	80

OPTION F INTERFACE WIRE LIST (Cont'd)

A5J2 PIN NO.	SIGNAL NAME	A2 PAD NO.
38	10^9 Bit "4" PRESET	62
39	10^9 Bit "8" PRESET	78
40	10^{10} Bit "8" PRESET	76
41	OPTION J INTERFACE	
42	OPTION J INTERFACE	
43	OPTION J INTERFACE	
44	OPTION J INTERFACE	
45	OPTION J INTERFACE	
46	OPTION J INTERFACE	
47	PRESET ENABLE	10
48	OPTION J INTERFACE	
49	OPTION J INTERFACE	
50	GROUND	34, 24, 66, 77

A parts list is not supplied or required for ordering information on the Option F, because the only additional non-standard part is the rear panel connector (A5J2), which is identified as follows;

A5J2 Connector, 50 pin Mfg. Amphenol, Mfg. No. 57-40500, EE No. 000433.

7.6 OPTION G AND G1

TO BE SUPPLIED

7.7 OPTION J

TO BE SUPPLIED

7.8 OPTION L

Option L provides for the addition of the Range 2 function to the standard Model 988/989 Microwave Counter. Range 2 provides for intermediate coverage from 25 MHz to 625 MHz with a input sensitivity of -7 dBm (100 mV rms) into a 50 ohm impedance. The optional L consists of an divide-by-four prescaler configured out of ECL logic that is added to the A1A1 PCB plug in Assembly and the required interconnect interface. All the documentation for Option L is provided for in Sections 1 thru 6 of this manual as a standard configuration. Thus no additional data is required or provided for in this section of the manual.

7.9 OPTION N

When Option N is incorporated into the standard instrument the relocation of the input RF connectors from the front panel to the rear panel is made to allow the Frequency Counter to be intergrated into a systems configuration. A degradation of up to 2 dBm from the standard input sensitivity specifications can be expected due to added cable lengths that are required.

Option N is configured by relocating the Range 1, 2, and 3 Input coax connectors (A4J1, A4J2, and A4J3) to pre-drilled mounting holes on the rear panel (refer to Figure 2-1 index 13, 14, and 15 for their panel locations). The input Range 1, 2 and 3 coax cables are replaced by Option N cables of greater length and the front panel input connector mounting holes are plugged by the use of "Butch" type hole plugs. Refer to the following parts parts list for the Option N cables and hole plugs when ordering replacements.

OPTION N PARTS LIST

REFERENCE	DESCRIPTION	MFG.	MFG. NO.	EI NO.	QTY
MP1 (N)	Plug, hole, .625 inch Dia.	HEYCO	P-625	007207	1
MP2, 3 (N)	Plug, hole, .375 inch Dia.	HEYCO	P-375	007206	2
W1 (N)	Coax Cable Assy., Range 3, Option N	EI		C-10854	1
W2 (N)	Coax Cable Assy., Range 2 Option N	EI		B-11024	1
W3 (N)	Coax Cable Assy., Range 1, Option N			B-11025	1

7.10 OPTION P

Option P provides a 41-line BCD output of the counters measurement data via a rear panel 50 pin connector (A5J1). The OUTPUT DATA Connector (A5J1) is an Amphenol 57-4500 dual line female connector which will mate to a Amphenol 57-3500 connector (plug) to allow for the interface to a remote device.

Internally the Option P is configured by adding a interface PCB Assembly, which consists of a extender card (EI part No. 006850) with a 50 pin 3VH25/1JN5 type Connector (EE part No. 006849) attached. This interface PCB Assembly provides for the connections between the Option P pins on the Counter Assembly A2 and the rear panel optional OUTPUT DATA connector A5J1. Installed on the Counter Assembly A2 as a standard configuration are 41 inverters that are arrayed by Hex Inverters IC's U1 thru U11 elements B thru E. These inverters convert the output data from false-to-positive true logic.

The following Option P interface list depicts the complete interface from the OUTPUT DATA connector A5J1 to the inverter or logic element. Located on the Counter Assembly PCB A2.

OPTION P INTERFACE LIST

A5J1 Pin No.	A2 Assy. Pin No.	A2 Assy. Logic Element	Function
1	26	U1C	10^0 Bit "1" Data
2	27	U1B	10^0 Bit "2" Data
3	28	U2C	10^1 Bit "1" Data
4	29	U2B	10^1 Bit "2" Data
5	30	U3C	10^2 Bit "1" Data
6	31	U3B	10^2 Bit "2" Data
7	32	U4C	10^3 Bit "1" Data
8	33	U4B	10^3 Bit "2" Data
9	34	U5C	10^4 Bit "1" Data
10	35	U5B	10^4 Bit "2" Data
11	36	U6C	10^5 Bit "1" Data
12	37	U6B	10^5 Bit "2" Data
13	38	U7C	10^6 Bit "1" Data
14	39	U7B	10^6 Bit "2" Data
15	40	U8C	10^7 Bit "1" Data
16	41	U8B	10^7 Bit "2" Data
17	42	U9C	10^8 Bit "1" Data
18	43	U9B	10^8 Bit "2" Data
19	44	U10C	10^9 Bit "1" Data
20	45	U10B	10^9 Bit "2" Data
21	46	U11C	10^{10} Bit "1" Data

OPTION P INTERFACE LIST (Cont'd)

A5J1 Pin No.	A2 Assy. Pin No.	A2 Assy. Logic Element	Function
22	22	Q25, U63A	+ Inhibit
23	23	Q30, Q31	Print Command
24	24		Ground
25	25		+ 5 V (REF)
26	1	U1D	10^0 Bit "4" Data
27	2	U1E	10^0 Bit "8" Data
28	3	U2D	10^1 Bit "4" Data
29	4	U2E	10^1 Bit "8" Data
30	5	U3D	10^2 Bit "4" Data
31	6	U3E	10^2 Bit "8" Data
32	7	U4D	10^3 Bit "4" Data
33	8	U4E	10^3 Bit "8" Data
34	9	U5D	10^4 Bit "4" Data
35	10	U5E	10^4 Bit "8" Data
36	11	U6D	10^5 Bit "4" Data
37	12	U6E	10^5 Bit "8" Data
38	13	U7D	10^6 Bit "4" Data
39	14	U7E	10^6 Bit "8" Data
40	15	U8D	10^7 Bit "4" Data
41	16	U8E	10^7 Bit "8" Data
42	17	U9D	10^8 Bit "4" Data
43	18	U9E	10^8 Bit "8" Data
44	19	U10D	10^9 Bit "4" Data
45	20	U10E	10^9 Bit "8" Data
46	21		N. C.
47	22	U36A	- Inhibit
48	23		N. C.
49	24		N. C.
50	25		Ground

NOTES

1. 10^0 is the least significant digit that is outputed and relates to the Hertz (Hz) units column of the instruments visual display.

2. The output binary data is in 1-2-4-8 BCD; positive zone positive true format, binary "0" = 0V, binary "1" = + 5V.

3. Print Command; is a positive going step at the end of the count cycle (0 volts to + 5 volts nominal). The Print Command is provided to signal the remote device that output data is preset for read out.

4. + Inhibit ($\geq$ 2 volts to 5 volts) when generated by the remote device will inhibit the storage transfer of the data and suppress the Print Command.

5. - Inhibit (0 volts) when generated by the remote device will inhibit the storage transfer of the data and suppress the Print Command.

6. The 10^{10} is the most significant digit and relates to the Giga Hertz (GHz) tens column of the visual display. This digit will indicate a decimal 0 or 1 (BCD Bit "1") only.

7.11 OPTION R5

Option R5 provides the necessary hardware for mounting the Model 988/989 Microwave Counter into a standard 19 inch relay rack. Installation of the Option R5 rack mount kit is outlined in the following step procedure and illustrated by figure 7-5. All necessary hardware with the exception of the screws for securing the completed assembly into the relay rack are supplied as part of the kit, and are listed in the following parts list.

OPTION R5 ASSEMBLY AND INSTALLATION PROCEDURE

STEP	ACTION
1	Secure the rack handles to each ear using the 10-32 3/8" FHMS screws (supplied).
2	Remove the four screws securing the side dress panels to the instrument chassis. These screws may be discarded.
3	With the four 6-32 1/2" FHMS screws (supplied) secure the rack ears to the side panels.
4	Secure the instrument into the rack and connect the required input, output and power cables.
	NOTE Rear panel clearance must be maintained to assure adequate air circulation, and the fan filter assembly must be unobstructed.

OPTION R5 PART LIST

Description	Mfg.	Mfg. No.	EI No.	Qty.
Rack Mounting Kit	EI	A-31-05558	045558	1
Handle Assy.	Litton Ind.	1006-12	000626	2
Ear Assy.	EI	B-05-04805	044805	2
Screw 10-32 3/8" FHMS	EI		003787	2
Screw 6-32 1/2" FHMS	EI		003774	4

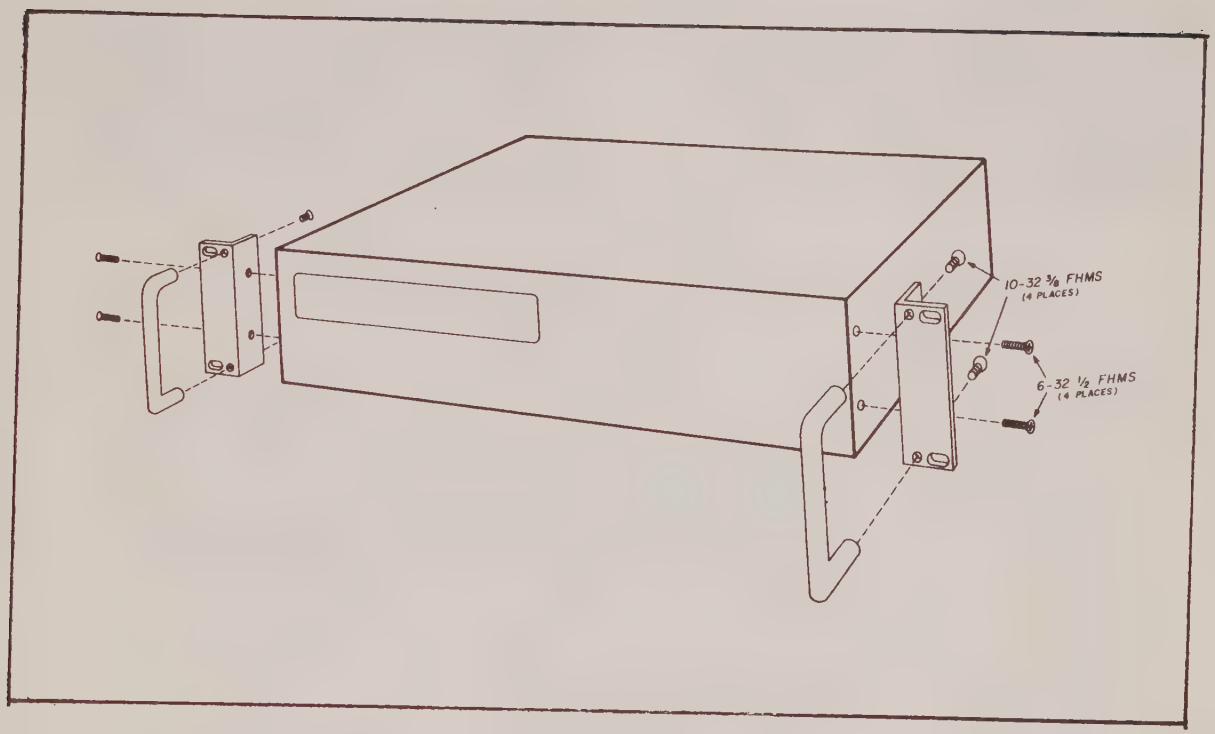


FIGURE 7-4 OPTION R5 RACK MOUNT ASSEMBLY

7.12 OPTION S

When the Option S is configured into the standard Microwave Counter a interface is provided to allow remote control of the Range 3 sweep start and stop frequencies by a BCD code via a rear panel 24 pin connector.

This Option is a systems orientated feature that allows shorter acquisition time when a known limited band width of measurements are to be made. The sweep search rate is ≃ 50 milli-seconds per GHz so if a 18 GHz signal is to be counted the normal acquisition time would be about 900 milli-seconds. If the sweep start frequency is preset to 17.6 GHz the time to acquire a 18 GHz signal would be ≃ 10 milli-seconds, thus providing an appreciable reduction in the acquisition time. If the Model 988/989 is to be configured as a sensor component of a data acquisition system the proper application of the Option S feature could reduce dead time by a appreciable amount.

The logic to support the sweep preset stop and start functions are included in the standard instrument's configuration and they share logic elements with the sweep generator counter located on PCB Assembly A1A3. For the detailed theory of operation of the sweep preset circuits refer to paragraph 3.3.11, page 3-20 of this manual.

The sweep START inputs relate to the three most significant digits of the digital sweep and is in effect the "N" preset start number. The least significant of the three (10^0) will always preset its BCD Bit "1" because its hard wired to ground (refer to Figure 6-8 logic element U14 pin 4). This insures that the sweep counter 10^0 DCU will always preset to an odd decimal number (1, 3, 5, 7 or 9). When the 10^0 DCU enters its first count it will output a (0, 2, 4, 6 or 8). These even decimal numbers relates to the 200 MHz step of the digital sweep.

The sweep STOP input relates to the three most significant digits of the digital sweep and is in effect the "N" preset stop number. The least significant digit of the three (10^0) is applied in BCD 2-4-8 format (Bit "1" being absent). This will insure that the preset stop frequency will have only even digits (0, 2, 4, 6 or 8) as its least significant decimal number. These even numbers relate to the 200 MHz step of the digital sweep.

The most significant digit (10^2) of both the START and STOP preset inputs are applied in a BCD 1-2 fromat (Bits "4" and "8" not applied). This allows the 10^2 digit to be a decimal 1, 2, or 3. The application of the bit "2" is superfluous because the upper limit of the YIG tuning is 18 GHz.

When Option S is installed a cable assembly with a 24 pin Amphenol 57-40240 connector (A5J3) on one end, faned out to two 14 pin connector is provided to configure the rear panel-to-A1A3 Assembly interface. The following wire list provides the interconnect data, pin numbers and part numbers of the cable assembly.

OPTION S WIRE LIST

Rear Pnl. Connector A5J3 Pin No.	Start Connector Pin No.	Stop Connector Pin No.	Function (Signal Name)
1	1		START 10^0 Bit "2"
2	2		START 10^0 Bit "4"
3	3		START 10^0 Bit "8"
4	4		START 10^1 Bit "1"
5	5		START 10^1 Bit "2"
6	6		START 10^1 Bit "4"
7	7		START 10^1 Bit "8"
8	8		START 10^2 Bit "1"
9	9		START 10^2 Bit "2"
10			N.C
11	10		PRESET ENABLE
12		12	+ 5 VOLTS
13		1	STOP 10^0 Bit "2"
14		2	STOP 10^0 Bit "4"
15		3	STOP 10^0 Bit "8"
16		4	STOP 10^1 Bit "1"
17		5	STOP 10^1 Bit "2"
18		6	STOP 10^1 Bit "4"
19		7	STOP 10^1 Bit "8"
20		8	STOP 10^2 Bit "1"
21		9	STOP 10^2 Bit "2"
22			N.C.
23			N.C.
24	14	14	GROUND

NOTES:

1. Rear panel connector A5J3 is a Amphenol 40240 24 pin connector, EI part number 000441

2. START and STOP connectors are Circuit Assy. Corp. CA-S-14P02-26-DO-012 Connector/Cable Assemblies modified, EI part number 007208.

3. The complete Option S Cable Assembly is an EI Assembly C-11349 and can be ordered as such.

4. The START and STOP BCD code is by contact closures or saturated NPN transistor to ground.

7.13 OPTION T

Option T provides for operation of the Microwave Counter on input power of 115/230 Vac 50-400 Hz. To install this option the standard Blower Assembly A5B1 is removed and replaced by a Blower Assembly A5B1 (T) which will operate on 115 Vac 50 to 400 Hz power. The rear panel fan cutout area is enlarged to accept the Option T Fan Assembly and a .22 MFD, 400V, 10% Mylar Capacitor is connected between connectors 1 and 2 of the fans terminal strip. A parts list is provided to identify and provide ordering information on the added component parts that make up Option T.

OPTION T PARTS LIST

Description	Mfg.	Mfg. No.	EI No.	Qty.
Fan, 115V, 50-400 Hz	ROTRON	SER 558YS	004909	1
Chassis, Fan	EI	C-11354	051352	1
Screen, Fan	EI	C-11354	051354	1
Filter, Fan Air	EI	B-11353	051353	1
Cover, Filter, Air	EI	C-11351	051351	1
Capacitor, .22 MFD, 400 WVDC, 10%, Mylar	SPRAGUE	150D Series	000224	1

MP MASTER
MA29720